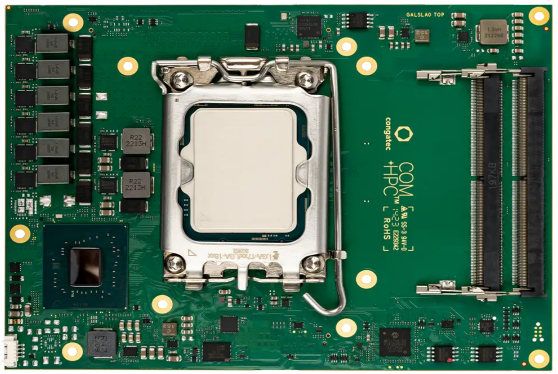


conga-HPC/cBLS

COM-HPC® 1.20 Client Size C Module with Intel® Core™ Processors (Series 2)

User's Guide

Revision 1.00

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Revision History

Revision	Date (yyyy-mm-dd)	Author	Changes
0.01	2026-06-01	RVI	• Preliminary release
0.02	2026-07-17	RVI	• Updated operating temperature definition in section 2.7 "Environmental Specifications" • Updated "Table 2 Commercial Variants (conga-HPC/cBLS)" • Added a note to section 2 "Specifications" regarding RAM capacity limitations applicable to several variants
1.00	2026-07-22	RVI	• Final release • Corrected the errorneous version number of the previous release

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Preface

This user's guide provides information about the components, features, connectors and system resources available on the conga-HPC/cBLS. It is one of three documents that should be referred to when designing a COM-HPC® application. The other reference documents that should be used include the following:

COM-HPC® Module Base Specification
COM-HPC® Carrier Design Guide

These documents can be found on the PICMG® website at www.picmg.org

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Note

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Terminology

Term	Description
DDI	Digital Display Interface
DTR	Dynamic Temperature Range
E-cores	Efficient-cores
eDP	Embedded DisplayPort
GB	Gigabyte
GHz	Gigahertz
HDA	High Definition Audio
kB	Kilobyte
kHz	Kilohertz
Mb	Megabit
MB	Megabyte
MHz	Megahertz
N.A	Not available
N.C	Not connected
PCH	Platform Controller Hub
PCIe	PCI Express
P-cores	Performance-cores
PEG	PCI Express Graphics
SATA	Serial ATA
TBD	To be determined
TDP	Thermal Design Power
TPM	Trusted Platform Module

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1 Introduction

1.1 COM-HPC® Concept

COM-HPC® is an open standard defined specifically for high performance Computer-on-Modules (COMs) for embedded systems. The defined module types are client module with fixed input voltage, client module with variable input voltage and server module with fixed input voltage.

The COM-HPC® modules are available in the following form factors:

- Mini 95 mm x 70 mm
- Size A 95 mm x 120 mm
- Size B 120 mm x 120 mm
- Size C 160 mm x 120 mm
- Side D 160 mm x 160 mm
- Side E 200 mm x 160 mm

Table 1 COM-HPC® Interface Summary

Features	Classification	Mini Module Min/Max	Client Module Min/Max	Server Module Min/Max	Comment
Ethernet	NBASE-T	1 / 2	1 / 2	1 / 1	
	KR/KX	N.A	0 / 2	2 / 8	
	SGMII	0 / 2	N.A	N.A	
Storage	SATA	0 / 2	0 / 2	0 / 2	Pin is shared with PCIe on mini module
PCIe	Lane 0-47	1 / 16	4 / 48	8 / 48	Two PCIe reference clock output pairs required on mini module
	Lane 48-63	N.A	N.A	0 / 16	
	BMC	N.A	0 / 1	1 / 1	
USB	USB 2.0 Ports 0-7	6 / 8	4 / 8	4 / 8	Ports 0-5 (mini module) or ports 0-3 (server/client module) are used for USB 3.2 and USB4 if implemented.
	USB 3.2 Gen 1 or Gen 2	0 / 5	0 / 4	0 / 4	Requires one SuperSpeed Tx pair and one Rx pair per port
	USB 3.2 Gen 2x2	0 / 4	0 / 4	0 / 2	Requires two SuperSpeed Tx pairs and two Rx pairs per port
	USB4	0 / 4	0 / 4	0 / 2	USB4 ports use USB 3.2 Gen 2x2 ports
SPI	eSPI	0 / 1	0 / 1	0 / 1	
	Boot SPI	1 / 1	1 / 1	1 / 1	
	General Purpose SPI	1 / 1	1 / 1	1 / 1	

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Features	Classification	Mini Module Min/Max	Client Module Min/Max	Server Module Min/Max	Comment
BIOS Select	-	1 / 1	1 / 1	1/1	
Display	DDI	0 / 2	1 / 3	N.A	Additional display outputs may be available on the USB4 interface. On mini module, DDI pins are shared with USB4.
	eDP	0 / 1	0 / 1	N.A	
MIPI	DSI	0 / 1	0 / 1	N.A	
	CSI	N.A [1]	0 / 2	N.A	[1] Optional FFC connectors for MIPI-CSI on the mini module.
Audio	Soundwire	0 / 2	0 / 2	N.A	I2S pins may be used for one HDA port or two additional SoundWire ports for a total of up to four SoundWire ports.
	I2S	0 / 1	0 / 1	N.A	
Other Serial Ports	I2C	2 / 3	2 / 2	2 / 2	I2C0 and I2C1 for client and server modules. The mini module supports a third I2C port (I2C2/MDIO for SGMII PHY setup).
	SMBus	1 / 1	1 / 1	1 / 1	
	IPMB	N.A	0 / 1	0 / 1	
	UART	0 / 2	0 / 2	1 / 2	
GPIO	-		12 / 12	12 / 12	
Miscellaneous	Watchdog Timer	0 / 1	0 / 1	0 / 1	
	Fan (PWM and tachometer)	1 / 1	1 / 1	1 / 1	
FuSa	FuSa set of signals	0 / 1	0 / 1	0 / 1	
Power Rails	VCC	12 / 12	28 / 28	28 / 28	
	VCC_5V-SBY	N.A	0 / 2	0 / 2	The mini module does not have 5V standby pins.
	VCC_RTC	1 / 1	1 / 1	1 / 1	
	GND	All	All	All	All available GND pins shall be used.
Connector	J1	1 / 1	1 / 1	1 / 1	
	J2	N.A	0 / 1	1 / 1	

1.2 The conga-HPC/cBLS

The conga-HPC/cBLS is a COM-HPC® client type size C module with Intel® Core™ (Series 2) processors. The conga-HPC/cBLS is based on the conga-HPC/cRLS platform and is equipped with two high performance connectors that ensure stable data throughput. It provides all the core functional requirements for any embedded application when mounted onto an application-specific carrier board. The new variants

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1.2.1 Options Information

The conga-HPC/cBLS is currently available in six commercial variants. The table below shows the different configurations available.

Table 2 Commercial Variants (conga-HPC/cBLS)

Part-No.		049820	049821	049822
Processor		Intel® Core™ 7 251E	Intel® Core™ 5 211E	Intel® Core™ 3 201E
Socket		FCLGA1700	FCLGA1700	FCLGA1700
P-Cores / E-Cores / Threads		8 / 16 / 32	6 / 4 / 16	4 / 0 / 8
P-Core Base / Max. Turbo Freq		2.1 GHz / 5.5 GHz	2.7 GHz / 4.9 GHz	3.6 GHz / 4.8 GHz
E-Core Base / Max. Turbo Freq		1.6 GHz / 4.4 GHz	2 GHz / 3.7 GHz	-- / --
Cache		36 MB Intel® Smart Cache	20 MB Intel® Smart Cache	12 MB Intel® Smart Cache
Processor Graphics		Intel® UHD Graphics 770 (32 EUs)	Intel® UHD Graphics 730 (24 EUs)	Intel® UHD Graphics 770 (24 EUs)
- Base / Max Dynamic Freq		300 MHz / 1.66 GHz	300 MHz / 1.55 GHz	300 MHz / 1.55 GHz
Memory Specifications		DDR5 up to 4000 MT/s	DDR5 up to 4000 MT/s	DDR5 up to 4000 MT/s
- Max Memory Size		up to 4x 48 GB (see caution below)	up to 4x 48 GB (see caution below)	up to 4x 48 GB (see caution below)
- # of Memory Channels		2 (Dual-Channel)	2 (Dual-Channel)	2 (Dual-Channel)
- ECC Memory Supported		Yes	Yes	Yes
Chipset		Intel® R680E	Intel® R680E	Intel® Q670E
PCIe® Lanes	Gen 3	14 lanes	14 lanes	10 lanes
	Gen 4	12 lanes	12 lanes	12 lanes
	Gen 5	16 lanes	16 lanes	16 lanes
Ethernet Controller		Intel® i226-LM	Intel® i226-LM	Intel® i226-V
- TSN Supported		Yes	Yes	No
CPU Use Condition [2]		PC/Client/Tablet, Workstation	PC/Client/Tablet, Workstation	PC/Client/Tablet
Processor Base Power/ Max. Turbo Power		65 W / N/A[2]	65 W / N/A[2]	60 W / N/A[2]

Part-No.	049830	049831	049832
Processor	Intel® Core™ 9 273PE	Intel® Core™ 7 253PE	Intel® Core™ 5 213PE
Socket	FCLGA1700	FCLGA1700	FCLGA1700
P-Cores / E-Cores / Threads	12 / 0 / 24	10 / 0 / 20	8 / 0 / 16
P-Core Base / Max. Turbo Freq	2.3 GHz / 5.4 GHz	2.5 GHz / 5.3 GHz	2.7 GHz / 5.2 GHz
Cache	36 MB Intel® Smart Cache	33 MB Intel® Smart Cache	24 MB Intel® Smart Cache
Processor Graphics	Intel® UHD Graphics 770 (32 EUs)	Intel® UHD Graphics 770 (32 EUs)	Intel® UHD Graphics 730 (24 EUs)
- Base / Max Dynamic Freq	300 MHz / 1.65 GHz	300 MHz / 1.65 GHz	300 MHz / 1.65 GHz
Memory Specifications	DDR5 up to 4000 MT/s	DDR5 up to 4000 MT/s	DDR5 up to 4000 MT/s

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Part-No.		049830	049831	049832
- Max Memory Size		up to 4x 16 GB (see caution below)	up to 4x 16 GB (see caution below)	up to 4x 16 GB (see caution below)
- # of Memory Channels		2 (Dual-Channel)	2 (Dual-Channel)	2 (Dual-Channel)
- ECC Memory Supported		Yes	Yes	Yes
Chipset		Intel® R680E	Intel® R680E	Intel® R680E
PCIe® Lanes	Gen 3	14 lanes	14 lanes	14 lanes
	Gen 4	12 lanes	12 lanes	12 lanes
	Gen 5	16 lanes	16 lanes	16 lanes
Ethernet Controller		Intel® i226-LM	Intel® i226-LM	Intel® i226-LM
- TSN Supported		Yes	Yes	Yes
CPU Use Condition [2]		PC/Client/Tablet, Workstation	PC/Client/Tablet, Workstation	PC/Client/Tablet
Processor Base Power/ Max. Turbo Power		65 W / N/A[2]	65 W / N/A[2]	65 W / N/A[2]

Note

1. *Intel® SoC use conditions. For more information, see Intel® documentation.*
2. *Intel® has not publicly released this information related to this processor variant.*

Caution

The standard conga-HPC/cBLS module's bottom-side SO-DIMM connectors exceed COM-HPC® height limitations. This design allows for increased system memory capacity but requires special carrier board design considerations:

- *Implement the 10 mm COM-HPC® carrier connector height stack option.*
- *Ensure components do not collide with the module's bottom-side SO-DIMM connectors, including during assembly.*

Failure to follow these design considerations may result in damage to the carrier board and module or cause improper fit.

For a COM-HPC® compliant conga-HPC/cBLS module without bottom-side SO-DIMM connectors, contact your congatec sales representative.

2 Specifications

2.1 Feature List

Table 3 Feature Summary

Form Factor	COM-HPC® Client Size C | Client Connector Pinout	
CPUs	Intel® Core™ processor (Series 2) - formerly codenamed: Bartlett Lake S	
Processor Socket	FCLGA 1700	
Chipset	R680E | Q670E	
DRAM	4 SO-DIMM sockets for DDR5 memory modules up to 48 GByte each | max. 192 GByte RAM system capacity [1] | up to 4000 MT/s | ECC Support [2]	
Graphics	Up to Intel® UHD Graphics 770 driven by Xᵉ Architecture | up to 32 EU	
Display	3x DDI | eDP	
Ethernet	2x 2.5 GbE with TSN support via Intel® i226 Ethernet controller series (TSN support is unavailable on PN 049822)	
I/O Interfaces	1x16 PCIe Gen 5 (PEG port) | 3x4 PCIe Gen 4 | up to 3x4 PCIe Gen 3 | 1x2 PCIe Gen3 | 4x USB 3.2 Gen2x2 (including 4x USB 2.0) + 4x USB2.0 | 2x SATA | 2x UART | 12x GPIO	
Audio	High-Definition Audio	
congatec Board controller	Multi-Stage Watchdog | non-volatile User Data Storage | Manufacturing and Board Information | Board Statistics I²C bus (fast mode, 400 kHz, multi-master) | Power Loss Control | Hardware Health Monitoring | POST Code redirection	
Embedded BIOS Feature	AMI Aptio® UEFI firmware | 32 Mbyte serial SPI with congatec Embedded BIOS feature | OEM Logo | OEM CMOS default settings | LCD Control | Display Auto Detection | Backlight Control | Flash Update	
Security	Trusted Platform Module (TPM 2.0)	
Power Management	ACPI 5.0a with battery support	
Operating Systems	Microsoft® Windows 11| Microsoft® Windows 11 IoT Enterprise | Microsoft® Windows 10 | Microsoft® Windows 10 IoT Enterprise | Linux | Yocto	
Hypervisor	conga-zones hypervisor	
Temperature	Operation: 0°C to +60°C	Storage: -20°C to +80°C
Relative Humidity	Operation: 10 to 85% r. H. non cond.	Storage: 5% to 85% r. H. non cond.
Size	120 x 160 mm	

Note

1. *Only up to 64 Gbyte RAM system capacity on PNs 049830, 049831, 049832. See section 1.2.1 "Options Information".*
2. *See the conga-HPC/cBLS Datasheet for more information regarding applicable SO-DIMM memory modules and ECC support.*

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2.2 Supported Operating Systems

The conga-HPC/cBLS supports the following operating systems:

- Microsoft® Windows 11
- Microsoft® Windows 11 IoT Enterprise
- Microsoft® Windows 10 IoT Enterprise 2021 LTSC
- Microsoft® Windows 10 Enterprise 2021 LTSC
- Linux
- Yocto
- RTS Hypervisor

Note

1. *The conga-HPC/cBLS supports only native UEFI Operating Systems. Legacy Operating Systems which require CSM (Compatibility Suppport Module) as part of the UEFI firmware are not supported anymore.*
2. *For Windows® 10 installation, we recommend a minimum storage capacity of 20 GB. congatec will not offer technical support for systems with less than 20 GB storage space.*
3. *To support Intel® i226 Ethernet controller in Linux by default, you need kernel 5.15 or higher.*

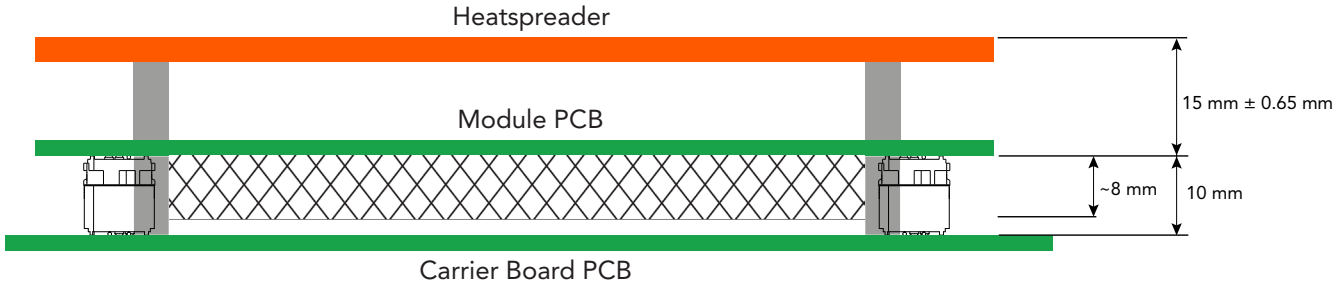
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2.3 Mechanical Dimensions

The standard conga-HPC/cBLS module variants have the following dimensions:

- length of 160 mm
- width of 120 mm
- PCB thickness of 2 mm +/- 10%

The overall height of an assembly with standard conga-HPC/cBLS module variants is shown below:



Note

3D models of congatec products are available at www.congatec.com/login. These models indicate the overall length, height and width of each product. If you need login access, contact your local sales representative.

Caution

The standard conga-HPC/cBLS module's bottom-side SO-DIMM connectors exceed COM-HPC® height limitations. This design allows for increased system memory capacity but requires special carrier board design considerations:

- *Implement the 10 mm COM-HPC® carrier connector height stack option.*
- *Ensure components do not collide with the module's bottom-side SO-DIMM connectors, including during assembly.*

Failure to follow these design considerations may result in damage to the carrier board and module or cause improper fit.

For a COM-HPC® compliant conga-HPC/cBLS module without bottom-side SO-DIMM connectors, contact your congatec sales representative.

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2.4 Supply Voltage Standard Power

The conga-HPC/cBLS requires 12 V DC ± 5 % input power (client module with fixed input voltage).

2.4.1 Electrical Characteristics

Power supply pins on the module's connectors limit the amount of input power. The following table provides an overview of the limitations for the conga-HPC/cBLS (client module with fixed input voltage).

Table 4 Input Power - Fixed 12 V In

Power Rail	Module Pin Current Capability (Ampere)	Input Range (V)	Min. Input (V)	Max. Module Input Power at Min. Input Voltage (W)	Assumed Conversion Efficiency (%)	Max. Module Load Power at Min. Input Voltage (W)
VCC	28 * 1.12 = 31.4	12V +/- 5%	11.4	358	85	304
VCC_5V_SBY	1.12	4.75 - 5.25	4.75	5.32	100	5.3 (with one VCC_5V_SBY pin) 10.6 (with two VCC_5V_SBY pins)
VCC_RTC	1.12	2.3 - 3.3	2.3			

2.4.2 Rise Time

The input voltages shall rise from 10 percent of nominal to 90 percent of nominal within a timeframe of 0.1 ms to 20 ms. The smooth turn-on requires that, during the 10 percent to 90 percent portion of the rise time, the slope of the turn-on waveform must be positive.

2.5 Power Consumption

The power consumption values were measured with the following setup:

- conga-HPC/cBLS
- modified congatec carrier board
- conga-HPC/cBLS cooling solution
- Microsoft® Windows® 10 (64-bit)

Note

The CPU was stressed to its maximum workload with the Intel® Power and Thermal Analysis Tool.

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The power consumption values were recorded during the following system states:

Table 5 Measurement Description

System State	Description	Comment
S0: Minimum value	Lowest frequency mode (LFM) with minimum core voltage during desktop idle	
S0: Maximum value	Highest frequency mode (HFM/Turbo Boost)	The CPU was stressed to its maximum frequency
S0: Peak current	Highest current spike during the measurement of "S0: Maximum value". This state shows the peak value during runtime.	Consider this value when designing the system's power supply to ensure that sufficient power is supplied during worst case scenarios
S3	COM is powered by VCC_5V_SBY	
S5	COM is powered by VCC_5V_SBY	
S5e	COM is powered by VCC_5V_SBY	

Note

1. *The fan and SATA drives were powered externally.*

2. *All other peripherals except a DP monitor were disconnected before measurement.*

The table below provides the power consumption values for the conga-HPC/cBLS at various system states:

Table 6 Power Consumption Values

Part No.	Memory Size	H.W Rev.	BIOS Rev.	CPU	Current (Ampere) (S0 @ 12V; S3, S5, S5e @ 5V)					
					S0: Min	S0: Max	S0: Peak	S3	S5	S5e
049820	4 x 32GB	B.0	GRLSR026	Intel® Core™ 7 251E	1.26	8.69	22.32	0.26	0.13	0.0008
049821	4 x 32GB	B.0	GRLSR026	Intel® Core™ 5 211E	1.00	5.82	12.56	0.26	0.13	0.0008
049822	4 x 32GB	B.0	GRLSR029	Intel® Core™ 3 201E	1.16	7.04	9.87	0.28	0.13	0.0008
049830	4 x 32GB	B.0	GRLSR028	Intel® Core™ 9 273PE	1.70	10.09	21.46	0.27	0.13	0.0008
049831	4 x 32GB	B.0	GRLSR030	Intel® Core™ 7 253PE	0.95	9.99	19.88	0.28	0.13	0.0008
049832	4 x 32GB	B.0	GRLSR030	Intel® Core™ 5 213PE	0.89	9.64	15.24	0.28	0.13	0.0008

Note

Power consumption values for other variants may be available on request. For more information, contact your local sales representative.

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2.6 Supply Voltage Battery Power

Table 7 CMOS Battery Power Consumption

RTC @	Voltage	Current
-10°C	3V DC	2.44 µA
20°C	3V DC	2.80 µA
70°C	3V DC	6.17 µA

Note

1. *Do not use the CMOS battery power consumption values listed above to calculate CMOS battery lifetime.*
2. *Measure the CMOS battery power consumption of your application in worst case conditions (for example, during high temperature and high battery voltage).*
3. *Consider the self-discharge of the battery when calculating the lifetime of the CMOS battery. For more information, refer to* https://wiki.congatec.com/wiki/RTC_Battery_Lifetime_(AN09).
4. *We recommend to always have a CMOS battery present when operating the conga-HPC/cBLS.*

2.7 Environmental Specifications

Temperature	Operation: 0° to 60°C	Storage: -20° to +80°C
Relative Humidity	Operation: 10% to 85%	Storage: 5% to 85%

Caution

The product is designed to operate in the above operating temperature range. It is the system integrator's responsibility to ensure that all components used on or with the product are operated within their individually specified temperature limits. For detailed information regarding the temperature specifications of individual components used on the product, refer to the respective thermal documentation (e.g., Hotspots CTNs) available in the customer login area at www.congatec.com *and/or the customer knowledge base* wiki.congatec.com. *Appropriate cooling measures must be implemented in the final application to ensure proper heat dissipation.*

Humidity specifications are for non-condensing conditions.

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2.8 Storage Specifications

This section describes the storage conditions that must be observed for optimal performance of congatec products.

2.8.1 Module

For long-term storage of the conga-HPC/cBLS (more than six months), keep the conga-HPC/cBLS in a climate-controlled building at a constant temperature between 5°C and 40°C, with humidity of less than 65% and at an altitude of less than 3000 m. Also ensure the storage location is dry and well ventilated.



Note

We do not recommend storing the conga-HPC/cBLS for more than five years under these conditions.

2.8.2 Cooling Solution

The heatpipes of congatec heatspreaders/cooling solutions are filled with water by default. For optimal cooling performance, do not store the heatspreaders/cooling solutions at temperatures below -20°C.



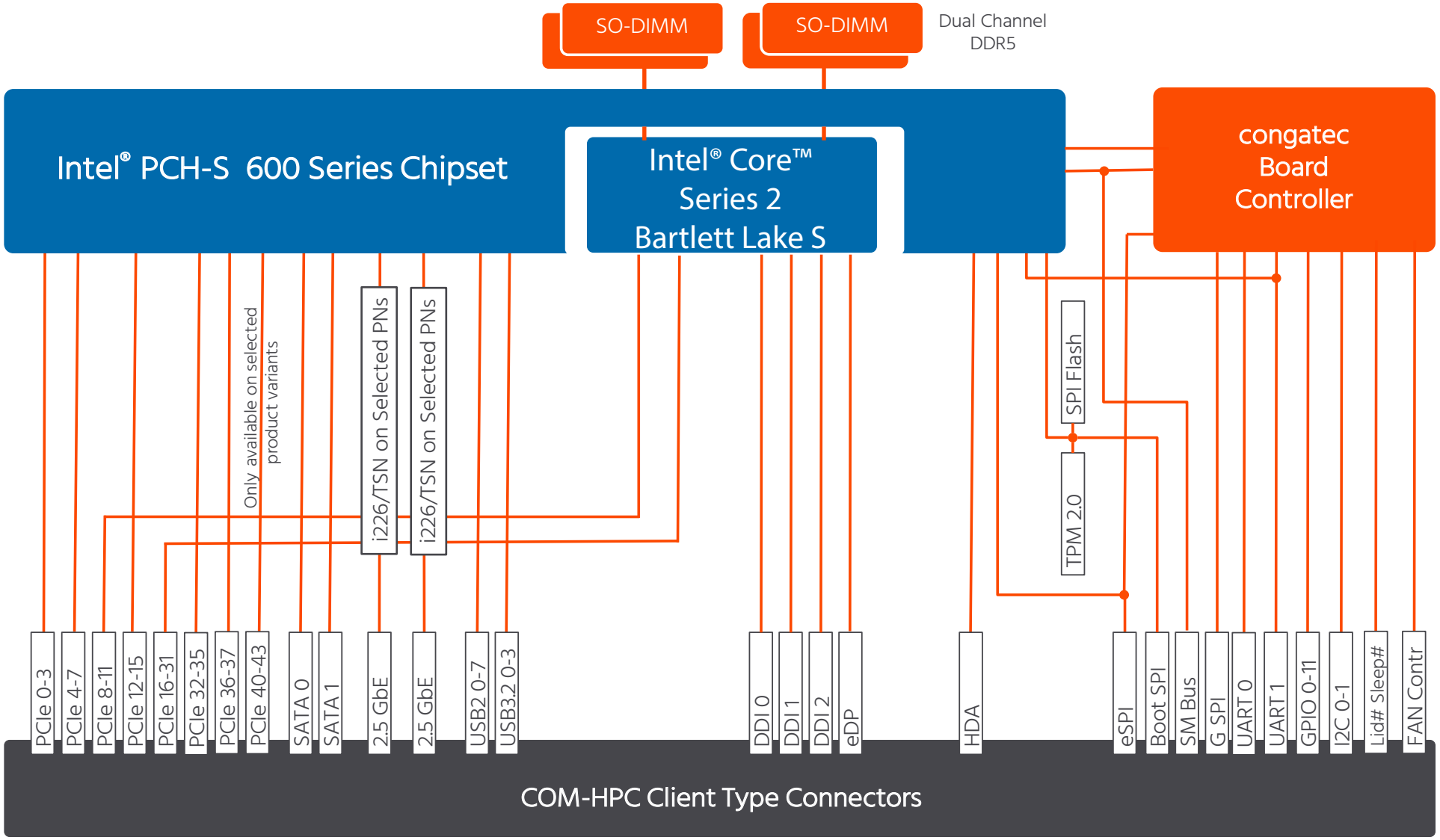
Caution

1. *For temperatures between -10°C and -20°C, preheat the heatpipes before operation. Optionally, the heatpipes can be filled with acetone instead. For more information, contact your local sales representative.*

2. *For optimal thermal dissipation, do not store the congatec cooling solutions for more than six months.*

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3 Block Diagram



4 Cooling Solutions

congatec GmbH offers the following cooling solutions for the conga-HPC/cBLS. The dimensions of the cooling solutions are shown in the sub-sections. All measurements are in millimeters.

Table 8 Cooling Solution Variants

Cooling Solution	Part No	Description
CSA	049650	Active cooling solution with 2.7 mm bore-hole standoffs
	049651	Active cooling solution with M2.5 threaded standoffs
HSP	049652	Heatspreader with 2.7 mm bore-hole standoffs
	049653	Heatspreader with M2.5 threaded standoffs
HPA	049654	Heatpipe adapter



Caution

1. *The congatec heatspreaders/cooling solutions listed above are tested only within the ambient temperature range of 0° to 55°C. Therefore, if your application that features one of the above congatec heat spreader/cooling solution operates outside this range, ensure the correct operating temperature of the module is maintained at all times. This may require additional cooling components for your final application's thermal solution.*

2. *The heatpipes of congatec heatspreaders/cooling solutions are filled with water by default. To ensure optimal cooling performance, they should not be stored at temperatures below -20°C. If the storage temperature drops below -10°C, the heatpipes should be pre-heated before operation. Optionally, the heatpipes can be filled with acetone instead.*

3. *For adequate heat dissipation, use the mounting holes on the cooling solution to attach it to the module. Apply thread-locking fluid on the screws if the cooling solution is used in a high shock and/or vibration environment. To prevent the standoff from stripping or cross-threading, use non-threaded carrier board standoffs to mount threaded cooling solutions.*

4. *For applications that require vertically-mounted cooling solution, use only coolers that secure the thermal stacks with fixing post. Without the fixing post feature, the thermal stacks may move.*

5. *Do not exceed the recommended maximum torque. Doing so may damage the module or the carrier board, or both.*

6. *Adequate cooling must be provided to ensure that the memory modules operate within the temperature limits specified in the respective vendor specifications. When memory modules are mounted in bottom sockets, additional airflow may be required to maintain compliance. Inadequate cooling can result in performance degradation, such as interface bandwidth reduction. Prolonged operation under inadequate cooling may ultimately lead to module failure.*

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Note

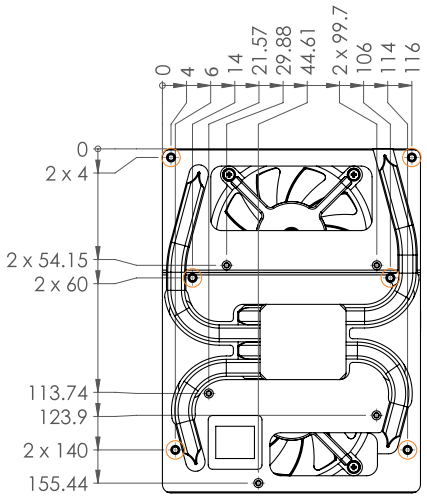
1. *We recommend a maximum torque of 0.4 Nm for carrier board mounting screws and 0.5 Nm for module mounting screws.*

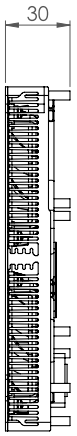
2. *The gap pad material used on congatec heat spreaders may contain silicon oil that can seep out over time depending on the environmental conditions it is subjected to. For more information about this subject, contact your local congatec sales representative and request the gap pad material manufacturer's specification.*

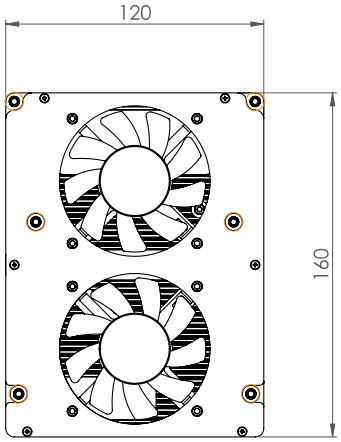
3. *For optimal thermal dissipation, do not store the congatec cooling solutions for more than six months.*

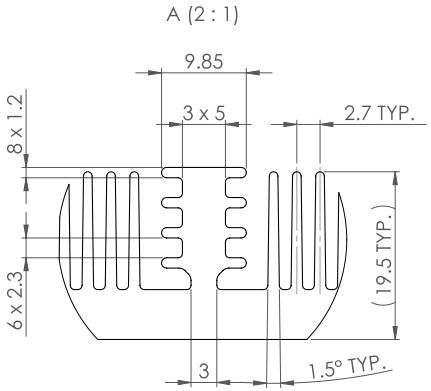
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4.1 CSA Dimensions

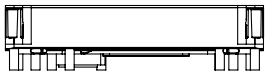




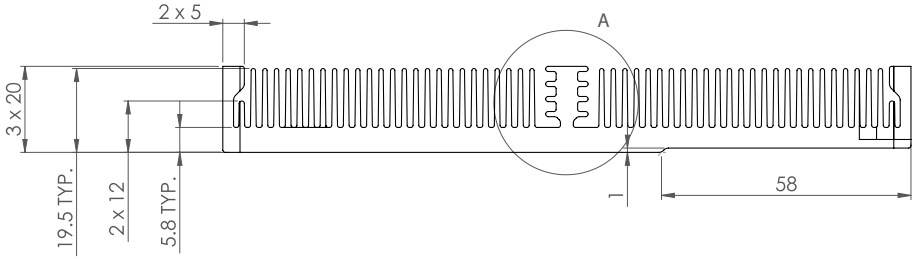


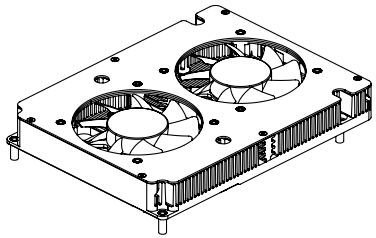


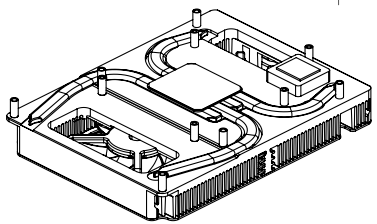
M2.5 x 11 mm
threaded standoff
for threaded version
or
ø2.7 x 11 mm
non-threaded standoff
for borehole version



HEAT SINK DESIGN
1 : 1

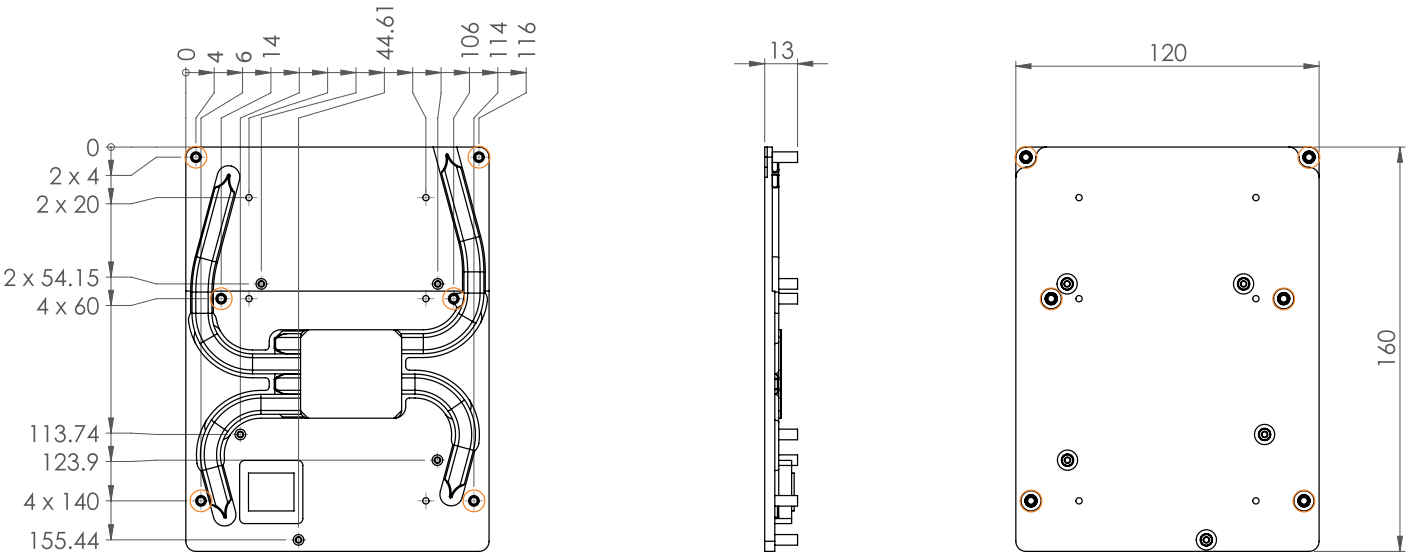






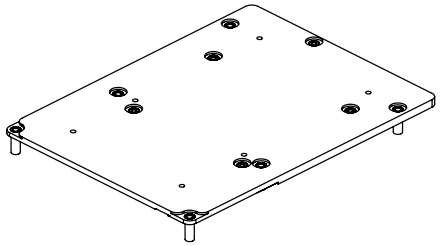
FIRST ANGLE
projection

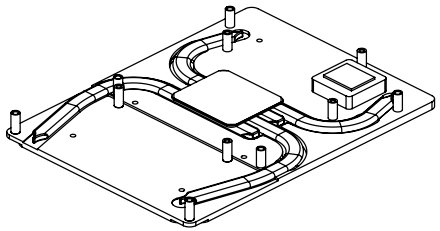
4.2 HSP Dimensions



M2.5 x 11 mm
threaded standoff
for threaded version
or
ø2.7 x 11 mm
non-threaded standoff
for borehole version



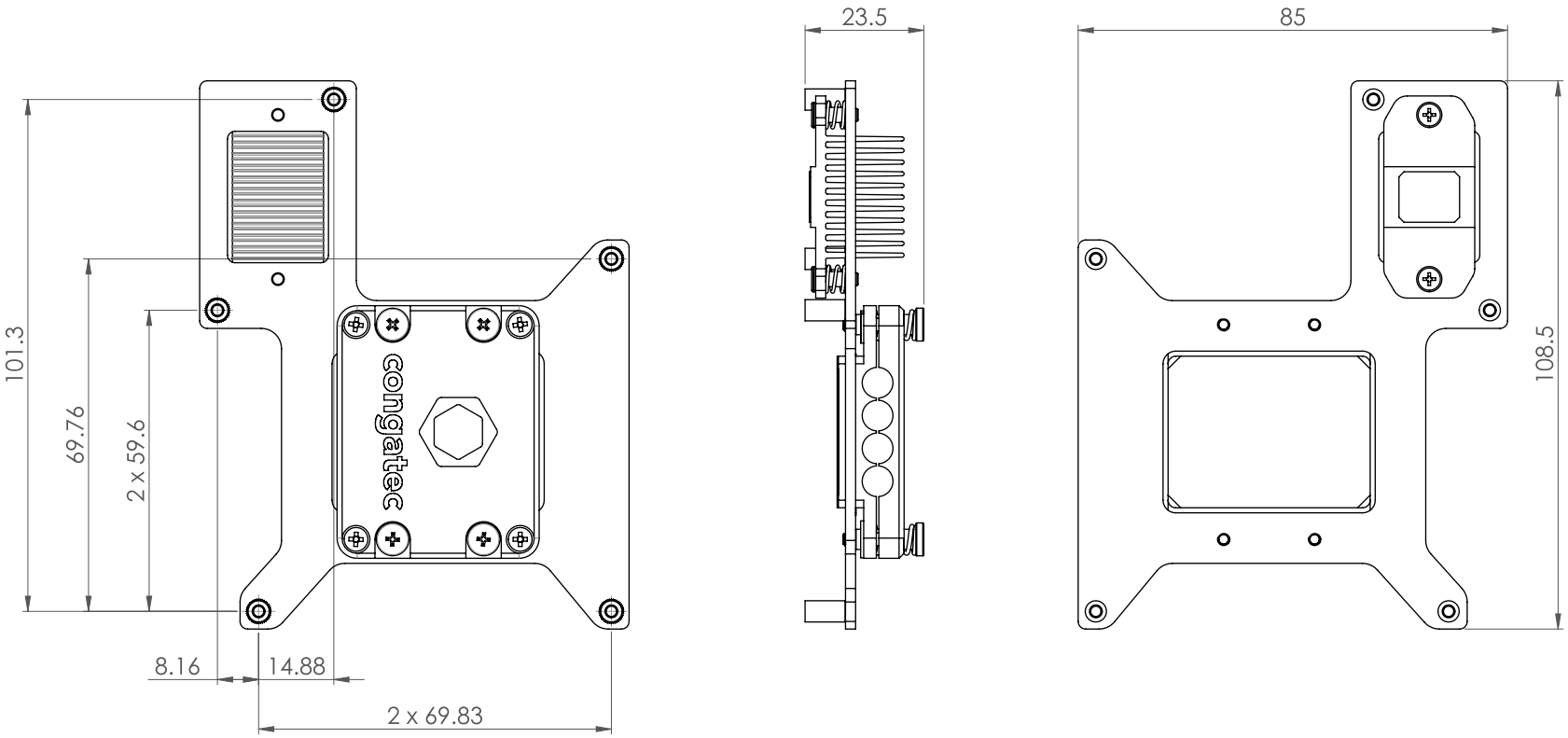


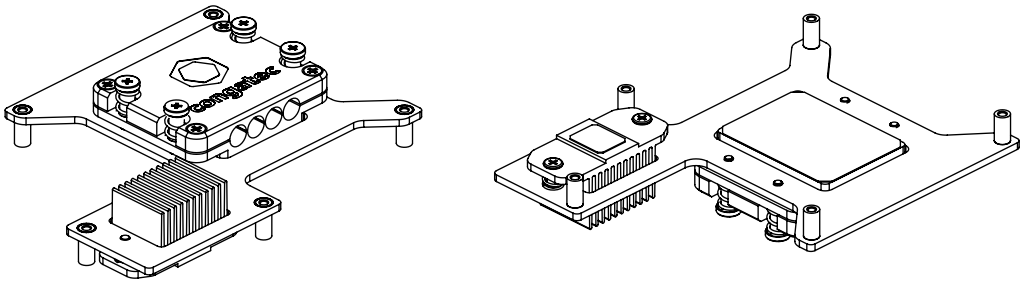


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4.3 HPA Dimensions



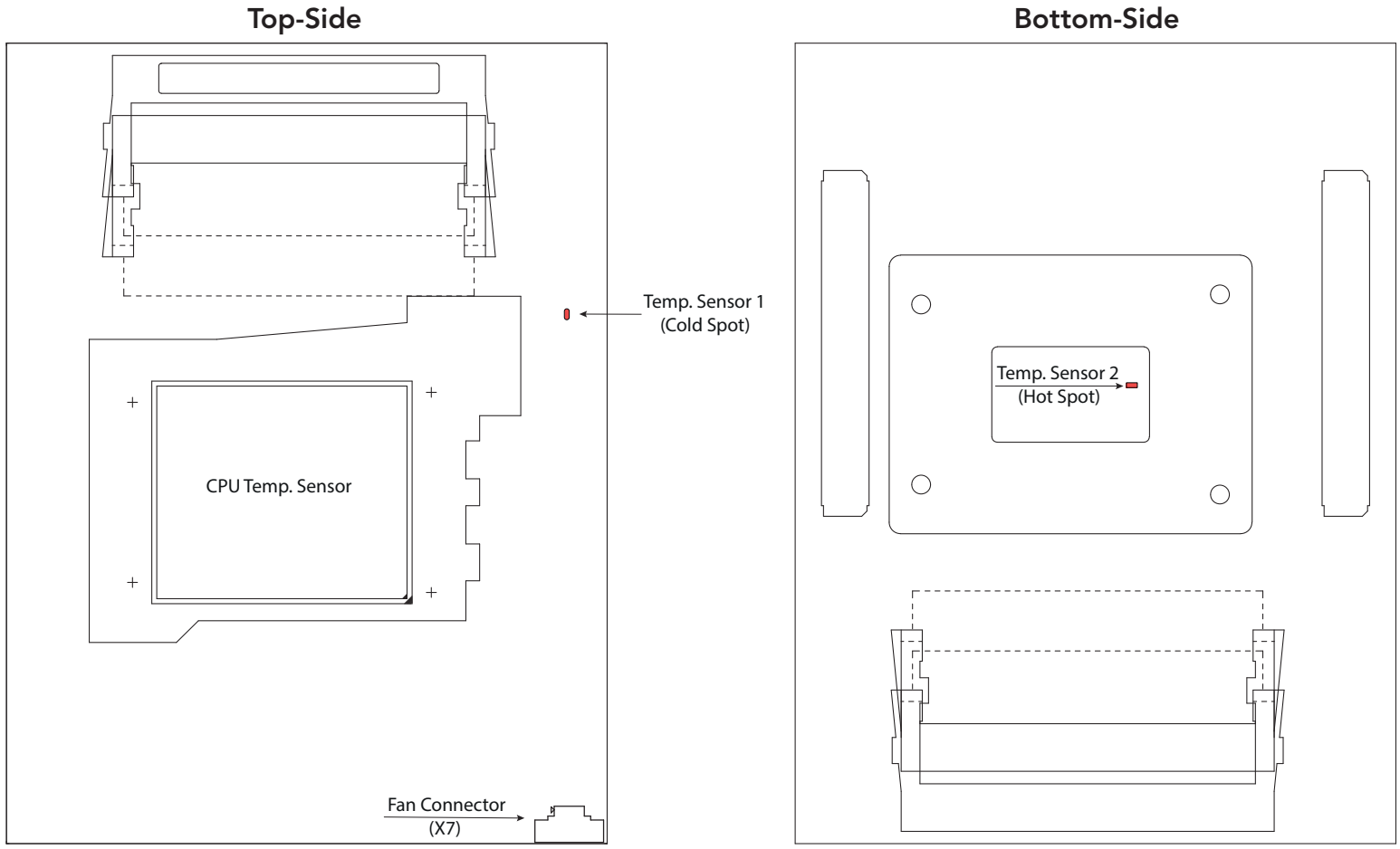


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5 Onboard Temperature Sensors

The conga-HPC/cBLS features two temperature sensors on the top-side and one temperature sensor on the bottom-side. The location of each sensor and the fan connector (X7) is indicated in the drawings below:



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6 Connector Rows

The conga-HPC/cBLS is connected to the carrier board via two 400-pin connectors (COM-HPC® Client Module pinout). These connectors are broken down into eight rows. The primary connector J1 consists of rows A, B, C, and D. The secondary connector J2 consists of rows E, F, G, and H. The following subsystems can be found on these connector rows.

6.1 NBASE-T Ethernet

The conga-HPC/cBLS offers two 2.5 Gigabit Ethernet interfaces (ETH[0:1]) via two onboard Intel® i226-LM/V controllers.[1] The interfaces support:

- full-duplex operation at 10/100/1000/2500 Mbps
- half-duplex operation at 10/100 Mbps
- Time-Sensitive Networking (TSN) [2]

Note

1. *The MAC address of the Intel i226 Ethernet controller is preprogrammed by default. The MAC address cannot be reprogrammed. If you require custom MAC address, contact your local sales representative.*
2. *Not supported in Windows® Operating Systems.*
3. *Only available on selected PNs as the Intel® i226-V Ethernet controller does not support TSN.*

6.2 Serial ATA

The conga-HPC/cBLS offers two Serial ATA interfaces (SATA[0:1]). The interfaces support:

- independent DMA operation
- SATA specification 3.2
- data transfer rates up to 6.0 Gb/s
- AHCI mode using memory space and RAID mode
- Hot-plug detect

Note

The interfaces do not support IDE legacy mode using I/O space.

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6.3 PCI Express (PCIe)

The conga-HPC/cBLS offers the following PCIe® lanes:

- up to 14 PCIe® Gen 3 lanes
- up to 12 PCIe® Gen 4 lanes
- up to 16 PCIe® Gen 5 lanes

The lanes support the link configurations listed in the table below:

Table 9 PCIe® Link Configurations

PCIe® Lane	PCIe® Generation (Max. Transfer Rate)	Link Configuration		COM-HPC® Grouping	Source	Comment
		Default	Optional			
PCIe00 - 03	Gen 3 (8 GT/s)	x1	x2, x4	Group 0 Low	Chipset	
PCIe04 - 07	Gen 3 (8 GT/s)	x1	x2, x4		Chipset	
PCIe08 - 11	Gen 4 (16 GT/s)	x4	-	Group 0 High	CPU	PEG port only supports Discrete Graphics (dGFx) and Storage Devices
PCIe12 - 15	Gen 4 (16 GT/s)	x4	x2		Chipset	
PCIe16 - 31	Gen 5 (32 GT/s)	x16	x8	Group 1	CPU	PEG port only supports Discrete Graphics (dGFx) and Storage Devices. Optional 2 x8 link configuration can be set in BIOS Setup: Advanced —> Misc —> PEG Port Configuration A customized BIOS is not required.
PCIe32 - 35	Gen 4 (16 GT/s)	x4	x1, x2	Group 2	Chipset	
PCIe36 - 37	Gen 3 (8 GT/s)	x1	x2		Chipset	
PCIe38 - 39	-	-	-		-	PCIe38 - 39 lanes are not available
PCIe40 - 43	Gen 3 (8 GT/s)	x4	x1, x2		Chipset	PCIe40 - 43 lanes are not available on variants with Intel® Q670E chipset. The optional link configurations are not required by the COM-HPC® Spec.

Note

Optional link configurations require a customized BIOS. Exception: PCIe16 - 31 (see comment for more details).

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6.4 USB Ports

The conga-HPC/cBLS offers up to:

- eight USB 2.0 ports
- four USB 3.2 Gen 2x2 ports

Note

For each USB 3.2 Gen 2x2 port, you need one USB 2.0 port with corresponding USB 3.2 SuperSpeed signals. Therefore, the available USB 2.0 ports depends on how many USB 3.2 ports you implement.

6.4.1 USB 2.0 Ports

The conga-HPC/cBLS offers up to eight USB 2.0 ports (USB[0:7]). The ports support:

- USB 2.0 specification
- High-Speed, Full-Speed and Low-Speed USB signaling
- data transfers of up to 480 Mbps (High-Speed mode)

6.4.2 USB 3.2 Ports

The conga-HPC/cBLS offers up to four USB 3.2 Gen 2x2 ports (USB[0:3]). The interfaces support:

- USB 3.2 specification
- wake up from S1-S4 sleep states (each wake up capable port must include USB 3.2 and USB 2.0 signaling)
- data transfers of up to 20 Gbps for USB 3.2 Gen 2x2 port (requires four differential signals and USB-C connector)
- SuperSpeed USB 20 Gbps, SuperSpeed USB 10 Gbps, SuperSpeed USB 5 Gbps, High-Speed, Full-Speed and Low-Speed traffic

Note

For each USB 3.2 Gen 2x2 port, you need one USB 2.0 port with corresponding USB 3.2 SuperSpeed signals. Therefore, the available USB 2.0 ports depends on how many USB 3.2 ports you implement.

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6.5 eSPI Interface

The conga-HPC/cBLS offers an eSPI interface for general purpose carrier board devices such as Super I/O, FPGAs, CPLDs and so on. The interface offers two chip select pins for carrier board devices.

Unlike the LPC interface, the eSPI interface runs from a 1.8 V supply.

Note

10 KΩ pull-up resistors have been added to 1.8 VSB on all eSPI_CS signals.

6.6 Boot SPI Interface

The conga-HPC/cBLS offers a Boot SPI interface for a carrier-based SPI BIOS flash device. The congatec onboard flash device (Winbond W25R256JV (256 Mb)) and TPM device (Infineon SLB9672) are also connected to this Boot SPI interface.

The pins to select the carrier-based SPI BIOS flash device are described in the section 6.7 "BIOS Boot Selection" below.

Note

1. *The power supply to the carrier board SPI (VCC_BOOT_SPI) is 3.3 V.*
2. *The onboard SPI flash is disabled when the carrier board SPI flash is enabled.*

6.7 BIOS Boot Selection

The boot select pins BSEL0-BSEL2 are configured to load the BIOS firmware from the conga-HPC/cBLS by default. Optionally, you can configure these pins to load the BIOS firmware from the carrier board SPI flash as described in the table below:

Table 10 BIOS Select Options

BSEL2	BSEL1	BSEL0	Boot Option
N.C	N.C	N.C	Boot from module SPI flash (default)
N.C	N.C	GND	Boot from carrier board SPI flash

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6.8 Display Interfaces

The conga-HPC/cBLS offers four dedicated display interfaces:

- three DP++ interfaces up to HBR3 (8.1 Gbps lane rate)
- one eDP™ interface up to HBR3 (8.1 Gbps lane rate)

The table below shows the supported display combinations and resolutions:

Table 11 Display Combinations and Resolutions

DDI0		DDI1		DDI2		eDP	
Interface	Max. Resolution	Interface	Max. Resolution	Interface	Max. Resolution	Interface	Max. Resolution
DP++	4096x2304 @ 60 Hz, 36 bpp	DP++	4096x2304 @ 60 Hz, 36 bpp	DP++	4096x2304 @ 60 Hz, 36 bpp	eDP	4096x2304 @ 60 Hz, 36 bpp

Note

A single DP display supports max. resolution of 7680 x 4320 @ 60Hz. A single eDP™ display supports max. resolution of 5120 x 3200 @ 120Hz. The actual display resolution dependents on several design factors and therefore may be lower on your system.

6.8.1 DisplayPort Dual-Mode (DP++)

The conga-HPC/cBLS offers three DP++ interfaces (DDI[0:2]). Each interface supports:

- VESA® DisplayPort™ Standard 2.1
- HDCP 2.3 and 1.4 content protection
- Various audio formats

6.8.2 Embedded DisplayPort (eDP)

The conga-HPC/cBLS offers one eDP™ interface. This interface supports:

- VESA® Embedded DisplayPort™ Standard 1.4b
- Spread-Spectrum Clocking
- eDP™ display authentication

Note

The eDP™ interface does not support HDCP.

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6.9 Camera Serial Interface (CSI) Ports

The conga-HPC/cBLS does not offer MIPI CSI input ports.

6.10 Audio Interfaces

The conga-HPC/cBLS offers the following audio interfaces:

- two MIPI SoundWire® serial audio ports
- one I²S format serial audio port
- one Intel® High Definition Audio (HDA) interface

Note

The SoundWire® and I2S audio ports are not verified because the respective Intel® drivers are currently not available. For a verified audio interface, we recommend to use HDA.

6.11 Asynchronous Serial Port Interfaces

The conga-HPC/cBLS offers two 16C550 compatible UART interfaces (UART[0:1]) via the congatec Board Controller. The interfaces support hardware handshake, flow control, and up to 115200 baud rate.

6.12 I²C Ports

The conga-HPC/cBLS offers two I²C ports (I2C[0:1]) via the congatec Board Controller with support for multi-master and fast mode.

Caution

I2C0 operates with 3.3V while I2C1 operates with 1.8V — as defined in the COM-HPC® Module Base Specification.

Note

1. *For the reserved I²C bus addresses, refer to section 10.3 "I2C".*
2. *You need the congatec CGOS driver and API to access the I²C interface.*

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6.13 Port 80 Support on USB_PD I2C Bus

The conga-HPC/cBLS offers BIOS Port 80h debug information over the USB Power Delivery I²C Bus (USB_PD_I2C_DAT and USB_PD_I2C_CLK). The debug information is serialized and must be deserialized on the carrier board. For information on how to deserialize and display the debug infromation on carrier board 7-segment displays, refer to the COM-HPC® Carrier Design Guide.

6.14 General Purpose SPI Port

The conga-HPC/cBLS offers a general purpose SPI port and two chip selects (GPSPI_CS[0:1]) via the congatec Board Controller by default.

Optionally, the general purpose SPI port can be provided via the Intel® chipset instead (assembly option).

6.15 SMBus

The conga-HPC/cBLS offers a System Management Bus (SMBus) via the Intel® chipset. The SMBus can be either always connected or isolated via a switch (BIOS Setup option).

Note

Make sure the address space of the carrier board SMBus devices does not overlap with the address space of the module devices. For the reserved SMBus addresses, refer to section 10.4 "SMBus".

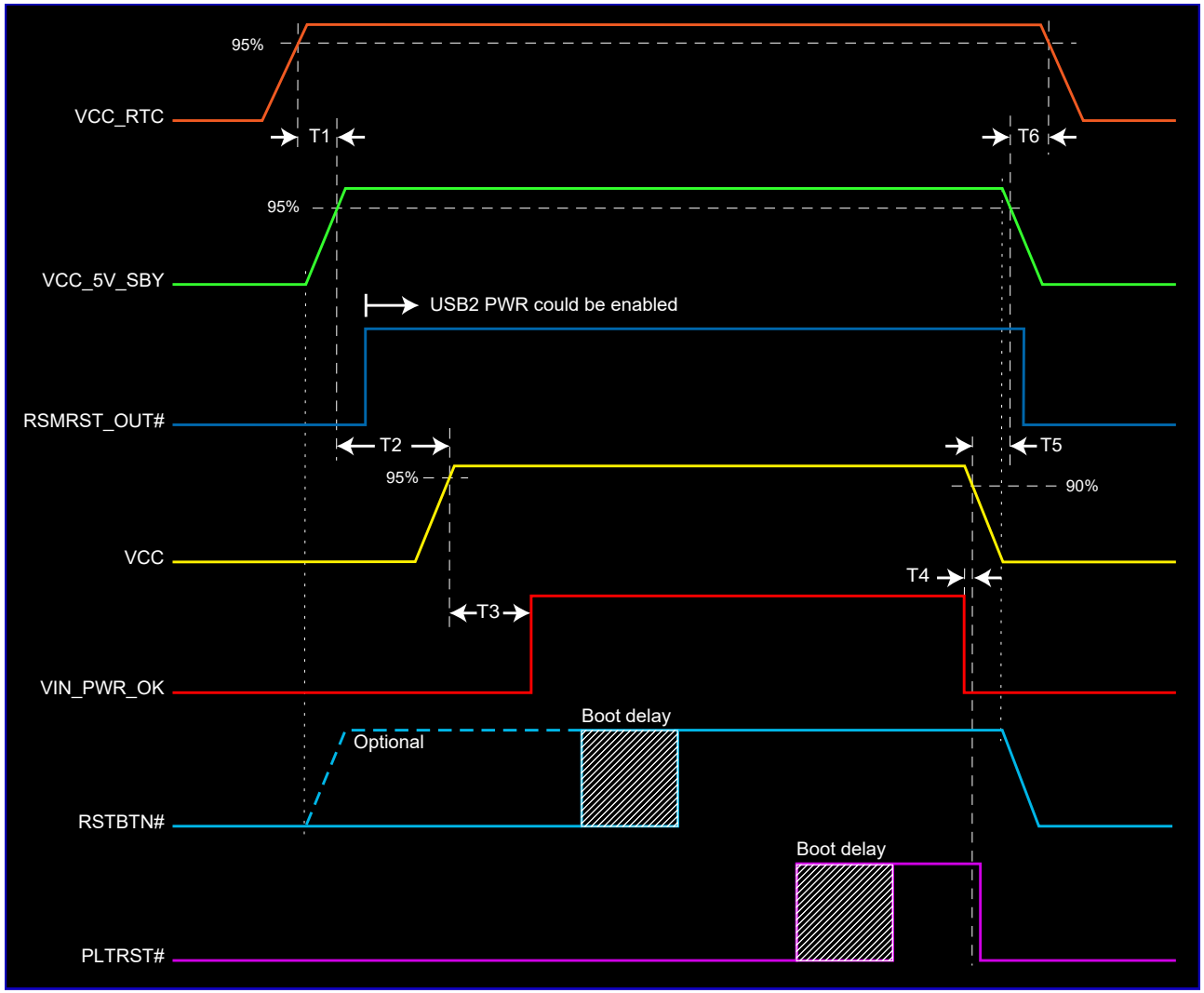
6.16 General Purpose Input Outputs (GPIOs)

The conga-HPC/cBLS offers 12 general purpose inputs and outputs (GPIO_[00:11]) via the congatec Board Controller.

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6.17 Power Control

The conga-HPC/cBLS operates with a fixed 12 V input voltage. Its power-up sequence is illustrated below:



T1-6 ≥ 0 ms

The power control signals VIN_PWR_OK, RSTBTN#, SUS_S3#, and PWRBTN# are described below. For more information, refer to the COM-HPC® Module Base Specification.

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VIN_PWR_OK

Power OK from main power supply or carrier board voltage regulator circuitry. A high value indicates that the power is good and the module can start its onboard power sequencing. Carrier board hardware should not drive VIN_PWR_OK low after the input power is stable. Hold RSTBTN# low instead to keep the module in a reset condition if necessary.

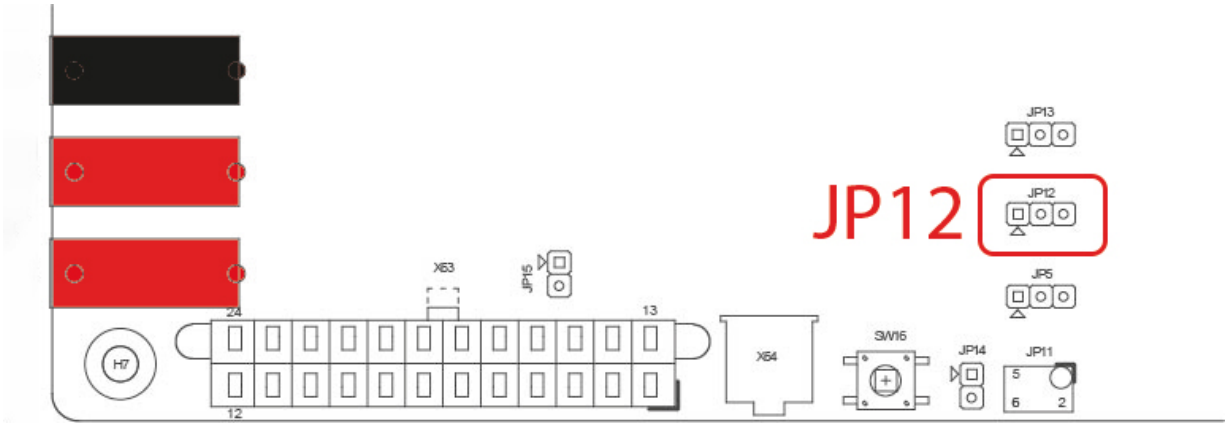
SUS_S3#

The SUS_S3# signal is an active-low output that can be used to turn on the main outputs of an ATX-style power supply. To accomplish this, invert the signal on the carrier board with an inverter or transistor that is supplied by standby voltage. With SUS_S3#, the conga-HPC/cBLS can control ATX-style power supplies.

Note

1. *If you do not use an ATX power supply, do not connect the conga-HPC/cBLS pins SUS_S3#, VCC_5V_SBY and PWRBTN#.*

2. *If you use an ATX power supply together with the conga-HPC/EVAL-Client, Revision A.1, evaluation carrier board, remove jumper JP12. Otherwise, the conga-HPC/cBLS will not start because the SUS_S3# signal is surpressed. The location of JP12 is indicated in the drawing below:*



PWRBTN#

When using ATX-style power supplies, PWRBTN# is used to connect to a momentary-contact, active-low debounced push-button input while the other terminal on the push-button must be connected to ground. This signal is internally pulled up to 3V_SB using a 100 kΩ resistor. When PWRBTN# is asserted it indicates that an operator wants to turn the power on or off. The response to this signal from the system may vary as a result of modifications made in BIOS settings or by system software.

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6.18 Inrush Current

The table below compares the inrush current and slew rate values of the conga-HPC/cBLS at different voltage ramp durations.

Table 12 Inrush Current

Power Rail	Inrush Current [A]	Slew Rate [kV/s]	Voltage Ramp [ms]	Comment
VCC	45.60	20.253	0.474	Worst-case scenario
VCC_5V_SBY	8.76	29.851	0.134	
VCC	10.68	8.421	1.140	Typical scenario
VCC_5V_SBY	1.18	3.361	1.190	

Note

Ensure the power supply and decoupling capacitors on the carrier board are adequate for proper power sequencing.

6.19 Power Management

ACPI

The conga-HPC/cBLS supports Advanced Configuration and Power Interface (ACPI) specification, revision 5.0a. It also supports Suspend to RAM (S3). For more information, see section 8.5 "ACPI Suspend Modes and Resume Events".

DEEP Sx

The Deep Sx is a lower power state employed to minimize the power consumption while in S3/S4/S5. In the Deep Sx state, the system entry condition determines if the system context is maintained or not. All power is shut off except for minimal logic which supports limited set of wake events for Deep Sx. The Deep Sx on resumption, puts system back into the state it is entered from. In other words, if Deep Sx state was entered from S3 state, then the resume path will place system back into S3.

S5e Power State

The conga-HPC/cBLS features a congatec proprietary Enhanced Soft-Off power state, described in section 7.2.4 "Enhanced Soft-Off State".

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7 Additional Features

The following additional features are available on the conga-HPC/cBLS.

7.1 Integrated Real-Time Hypervisor

The RTS Hypervisor is integrated into the congatec firmware on the conga-HPC/cBLS by default. With the RTS Hypervisor, you can consolidate functionality that previously required multiple dedicated systems on a single x86 hardware platform.

The integrated RTS Hypervisor offers a 30-day free evaluation license. The 30-day evaluation starts when the customer receives the x86-based modules. To access the full package, contact congatec Sales team via the online "Request Quote" button for your particular product at https://www.congatec.com/en/products/hypervisor-products/.

To activate the RTS Hypervisor, change the “Boot Device” in the BIOS setup menu to “Integrated RTS Hypervisor”.

1. Press F2 or DEL during POST to enter the BIOS setup menu.
2. Go to the Boot tab to enter the Boot setup screen.
3. Select “Integrated RTS Hypervisor" as “1st Boot Device”.
4. Go to the Save & Exit tab and select “Save Changes and Exit”.

For more information about the integrated Hypervisor, refer to https://wiki.congatec.com/wiki/Hypervisor_on_Module_(AN56).

Note

1. *The configuration steps and the BIOS setup menu above are valid for "Type Based Boot Priority". For "UEFI Boot Priority", the BIOS setup menu may differ.*
2. *The Real-Time Operating System images, driver packages for the General-Purpose Operating System and the installation procedures for the Operating Systems are available for download under the "Technical information" section, in the restricted area of congatec website at www.congatec.com/login. If you require login access, contact your local sales representative.*

7.2 congatec Board Controller (cBC)

The conga-HPC/cBLS is equipped with a Microchip microcontroller. This onboard microcontroller plays an important role for most of the congatec embedded/industrial PC features. It fully isolates some of the embedded features such as system monitoring or the I²C bus from

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the x86 core architecture, which results in higher embedded feature performance and more reliability, even when the x86 processor is in a low power mode. It also ensures that the congatec embedded feature set is fully compatible amongst all congatec modules.

The congatec Board Controller (cBC) supports the following features:

- Board information (See section 7.2.1)
- Watchdog (See section 7.2.2)
- Asynchronous Serial Port Interfaces (See section 6.11)
- I²C Ports (See section 6.12)
- Port 80 Support on USB_PD I2C Bus (See section 6.13)
- General Purpose SPI Port (See section 6.14)
- SMBus (See section 6.15)
- General Purpose Input Outputs (GPIOs) (See section 6.16)
- Fan Control (See section 7.2.3)
- Enhanced Soft-Off State (See section 7.2.4)
- Power Loss Control (See section 7.2.5)

7.2.1 Board Information

The cBC provides a rich data-set of manufacturing and board information such as serial number, EAN number, hardware and firmware revisions, and so on. It also keeps track of dynamically changing data like runtime meter and boot counter.

7.2.2 Watchdog

The cBC provides a multi stage watchdog solution that is triggered by software. For more information about the Watchdog feature, refer to https://wiki.congatec.com/wiki/Watchdog_(AN03).

7.2.3 Fan Control

The cBC provides signals for a primary and secondary fan. Signals for the primary fan are routed to onboard connector X7. Signals for the secondary fan are routed to the COM-HPC® connector.

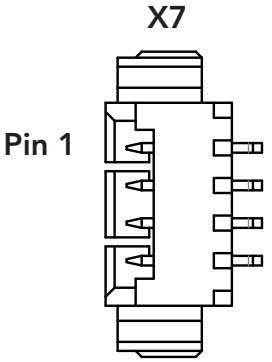
For the location of the onboard connector and information about the temperature sensors, see section 5 "Onboard Temperature Sensors".

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The pinout of the primary fan connector (X7) is described in the table below:

Table 13 Primary Fan Connector (X7) Pinout

Pin	Signal
1	GND
2	+12V_FAN
3	CPU_FAN_TACHIN
4	CPU_FAN_PWMOUT



Connector Type

X7: 4x1 pins, 1.25mm pitch (Molex 53261-0471); Possible Mating Connector: Molex 51021-0400

Note

A four wire fan must be used to generate the correct speed readout.

7.2.4 Enhanced Soft-Off State

The cBC provides an enhanced Soft-Off state (S5e)—a congatec proprietary low-power Soft-Off state. In this state, the CPU module switches off almost all the onboard logic to reduce the power consumption to absolute minimum (between 0.8 mA and 1 mA).

The S5e supports power button, sleep button and SMBALERT# wake events. For detailed description of the S5e state, refer to https://wiki.congatec.com/wiki/S5e_Implementation_(AN36).

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7.2.5 Power Loss Control

The cBC provides the power loss control feature. The power loss control feature determines the behaviour of the system after an AC power loss occurs. This feature applies to systems with ATX-style power supplies which support standby power rail.

The term "power loss" implies that all power sources, including the standby power are lost (G3 state). Once power loss (transition to G3) or shutdown (transition to S5) occurs, the board controller continuously monitors the standby power rail. If the standby voltage remains stable for 30 seconds, the cBC assumes the system was switched off properly. If the standby voltage is no longer detected within 30 seconds, the module considers this an AC power loss condition.

The power loss control feature has three different modes that define how the system responds when standby power is restored after a power loss occurs. The modes are:

- Turn On: The system is turned on after a power loss condition
- Remain Off: The system is kept off after a power loss condition
- Last State: The board controller restores the last state of the system before the power loss condition

Note

1. *If a power loss condition occurs within 30 seconds after a regular shutdown, the cBC may incorrectly set the last state to "ON".*
2. *The settings for power loss control have no effect on systems with AT-style power supplies which do not support standby power rail.*
3. *The 30 seconds monitoring cycle applies only to the "Last State" power loss control mode.*

7.3 OEM BIOS Customization

The conga-HPC/cBLS is equipped with congatec Embedded BIOS, which is based on American Megatrends Inc. Aptio UEFI firmware. The congatec Embedded BIOS allows system designers to modify the BIOS. For more information about customizing the congatec Embedded BIOS, refer to the congatec System Utility user's guide: https://wiki.congatec.com/wiki/Congatec_System_Utility_-_CGUTIL or contact technical support.

The supported customization features are described in the following sub-sections.

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7.3.1 OEM Default Settings

This feature allows system designers to create and store their own BIOS default configuration. Customized BIOS development by congatec for OEM default settings is no longer necessary because customers can easily perform this configuration by themselves using the congatec system utility CGUTIL. For information on how to add OEM default settings to the congatec Embedded BIOS, refer to https://wiki.congatec.com/wiki/Create_OEM_Default_Map_(AN08).

7.3.2 OEM Boot Logo

This feature allows system designers to replace the standard text output displayed during POST with their own BIOS boot logo. Customized BIOS development by congatec for OEM Boot Logo is no longer necessary because customers can easily perform this configuration by themselves using the congatec system utility CGUTIL. For information on how to add an OEM boot logo to the congatec Embedded BIOS, refer to https://wiki.congatec.com/wiki/Create_and_add_a_Boot_Logo_(AN11).

7.3.3 OEM POST Logo

This feature allows system designers to replace the congatec POST logo displayed in the upper left corner of the screen during BIOS POST with their own BIOS POST logo. Use the congatec system utility CGUTIL 1.5.4 or later to replace/add the OEM POST logo.

7.3.4 OEM DXE Driver

This feature allows designers to add their own UEFI DXE driver to the congatec embedded BIOS. Contact congatec technical support for more information on how to add an OEM DXE driver.

7.4 congatec Battery Management Interface

To facilitate the development of battery powered mobile systems based on embedded modules, congatec GmbH defined an interface for the exchange of data between a CPU module (using an ACPI operating system) and a Smart Battery system. A system developed according to the congatec Battery Management Interface Specification can provide the battery management functions supported by an ACPI capable operating system (for example, charge state of the battery, information about the battery, alarms/events for certain battery states and so on) without the need for additional modifications to the system BIOS.

In addtion to the ACPI-Compliant Control Method Battery mentioned above, the latest versions of the conga-HPC/cBLS BIOS and board controller firmware also support LTC1760 battery manager from Linear Technology and a battery only solution (no charger). All three battery solutions are supported on the I²C bus and the SMBus. This gives the system designer more flexibility when choosing the appropriate battery sub-system. For more information about the supported Battery Management Interface, contact your local sales representative.

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7.5 API Support (CGOS)

In order to benefit from the above mentioned non-industry standard feature set, congatec provides an API that allows application software developers to easily integrate all these features into their code. The CGOS API (congatec Operating System Application Programming Interface) is the congatec proprietary API that is available for all commonly used Operating Systems such as Win32, Win64, Win CE, Linux. The architecture of the CGOS API driver provides the ability to write application software that runs unmodified on all congatec CPU modules. All the hardware related code is contained within the congatec embedded BIOS on the module. See section 1.1 of the CGOS API software developers guide, available at www.congatec.com.

7.6 Security Features

The conga-HPC/cBLS is equipped with an onboard SPI TPM 2.0 (Infineon SLB9672).

7.7 Suspend to Ram

The conga-HPC/cBLS supports the power saving mode Suspend to RAM (S3).

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8 conga Tech Notes

The conga-HPC/cBLS has some technological features that require additional explanation. The following section will give the reader a better understanding of some of these features.

8.1 Adaptive Thermal Monitor and Catastrophic Thermal Protection

Intel® Xeon, Core™ i9/i7/i5/i3 and Celeron® processors have a thermal monitor feature that helps to control the processor temperature. The integrated TCC (Thermal Control Circuit) activates if the processor silicon reaches its maximum operating temperature. The activation temperature that the Intel® Thermal Monitor uses to activate the TCC can be slightly modified via TCC Activation Offset in BIOS setup submenu "CPU submenu".

The Adaptive Thermal Monitor controls the processor temperature using two methods:

- Adjusting the processor's operating frequency and core voltage (EIST transitions)
- Modulating (start/stop) the processor's internal clocks at a duty cycle of 25% on and 75% off

When activated, the TCC causes both processor core and graphics core to reduce frequency and voltage adaptively. The Adaptive Thermal Monitor will remain active as long as the package temperature remains at its specified limit. Therefore, the Adaptive Thermal Monitor will continue to reduce the package frequency and voltage until the TCC is de-activated. Clock modulation is activated if frequency and voltage adjustments are insufficient. Additional hardware, software driver, or operating system support is not required.

Intel® Core™ i7/i5/i3, Celeron® and Pentium® processors use the THERMTRIP# signal to shut down the system if the processor's silicon reaches a temperature of approximately 125°C. The THERMTRIP# signal activation is completely independent from processor activity and therefore does not produce any bus cycles.

Note

1. *For THERMTRIP# to switch off the system automatically, use an ATX style power supply.*

2. *The maximum operating temperature for Intel® Xeon, Core™ i9/i7/i5/i3, and Celeron® processors is 100°C.*

3. *To ensure that the TCC is active for only short periods of time, thus reducing the impact on processor performance to a minimum, it is necessary to have a properly designed thermal solution. The Intel® Xeon, Core™ i9/i7/i5/i3, and Celeron® processor's respective datasheet can provide you with more information about this subject.*

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8.2 Processor Performance Control

8.2.1 Enhanced Intel SpeedStep Technology (EIST)

The operating system can manage and choose P-states using the Enhanced Intel® SpeedStep® Technology. This technology offers several key features, including multiple frequencies and voltage points that optimize performance and power efficiency. These operating points are referred to as P-states, and frequency selection is software-controlled by writing to processor model-specific registers (MSRs). The voltage is adjusted based on the selected frequency and the number of active IA cores. Once established, the phase locked loop (PLL) locks onto the target frequency, which is shared by all active IA cores with the same voltage.

In a multi-core processor, the highest frequency P-state requested by any active IA core is selected. Software-requested transitions are permitted at any time, but if a previous transition is in progress, the new transition is deferred until the previous one is completed. The processor internally controls voltage ramp rates to ensure smooth transitions without glitches.

8.2.2 Intel Speed Shift Technology

Intel® Speed Shift Technology is an energy-saving approach to frequency control that relies on hardware rather than operating system control. The operating system is informed of the hardware P-states that are available and can either request a specific P-state or allow the hardware to determine the P-state.

The request made by the operating system is based on the workload requirements and knowledge of the processor's capabilities. Meanwhile, the processor's decision is influenced by various system constraints, such as workload demand, thermal limits, and the minimum and maximum levels of performance requested by the operating system, while taking into account the activity window.

8.2.3 Intel Turbo Boost Technology 2.0

The IA core/processor graphics core of the processor can automatically run faster than its base frequency, using the Intel® Turbo Boost Technology 2.0. This feature operates within power, temperature, and current limits and optimizes performance for both single-threaded and multi-threaded workloads.

With Intel® Turbo Boost Technology 2.0, the application power is directed more towards Thermal Design Power (TDP). The processor can exceed the TDP by going as high as PL2 for short durations. However, if the cooling solution is not designed accordingly, the system may face performance and thermal issues as more applications will run at the maximum power limit for extended periods. For more information about Intel® Turbo Boost 2.0 Technology visit the Intel® website.

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8.2.4 Intel Performance Hybrid Architecture

The Intel® Performance Hybrid Architecture comprises two core types, namely P-Cores and E-Cores:

- P-Cores refer to performance cores
- E-Cores refer to efficient cores

Both P-Cores and E-Cores utilize the same instruction set and model-specific registers (MSRs). However, when hybrid computing is enabled, the available instruction sets are fewer than those available to P-Cores. The processor algorithm determines the frequency of both P-Cores and E-Cores to optimize performance and power usage. The Intel® Performance Hybrid Architecture architecture is optimized for a wide range of workload types, including:

- single threaded
- partially threaded
- multi threaded

For more information about Intel® Performance Hybrid Architecture, refer to the Intel® website:

https://www.intel.com/content/www/us/en/developer/articles/technical/hybrid-architecture.html

8.3 Intel® Virtualization Technology

Intel® Virtualization Technology (Intel® VT) makes a single system appear as multiple independent systems to software. With this technology, multiple, independent operating systems can run simultaneously on a single system. The technology components support virtualization of platforms based on Intel® architecture microprocessors and chipsets. Intel® Virtualization Technology for Intel® 64 and Intel® Architecture (Intel® VT-x) added hardware support in the processor to improve the virtualization performance and robustness.

RTS Real-Time Hypervisor supports Intel® VT and is verified on all current congatec x86 hardware.

Note

congatec supports RTS Hypervisor.

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8.4 Thermal Management

ACPI is responsible for allowing the operating system to play an important part in the system's thermal management. This results in the operating system having the ability to implement cooling decisions according to the demands of the application.

The conga-HPC/cBLS offers hardware-based support for passive and active cooling. Passive cooling is implemented in the Intel CPU via the Thermal Control Circuit (TCC) Activation Offset setting in the CPU configuration setup sub-menu. The TCC in the processor is activated at 100°C by default but can be lowered by the Activation Offset—for example, an activation offset of "10" will activate TCC at 90°C. ACPI OS support is not required. See section 8.1 "Adaptive Thermal Monitor and Catastrophic Thermal Protection" for more information.

The congatec Board Controller (cBC) supports active cooling solution. The cBC controls the fan's speed based on the temperature readings of the CPU. This feature does not require ACPI OS support. The only software-controlled thermal trip point on conga-HPC/cBLS is the Critical Trip Point. The active or passive cooling policy should ensure that the CPU temperature does not reach this trip point. However, if the critical trip point is reached, the OS will shut down properly in order to prevent damage to the system. Use the "critical trip point" setup node in the BIOS setup menu to determine the temperature threshold at which the system shuts down.

Note

The Automatic Critical Trip Point BIOS setting shuts down the system at 5°C above the maximum specified temperature of the processor.

8.5 ACPI Suspend Modes and Resume Events

The conga-HPC/cBLS BIOS supports S3 (Suspend to RAM), S4 (Suspend to Disk) and S5 (Soft-Off). The table below lists the events that wake the system from S3.

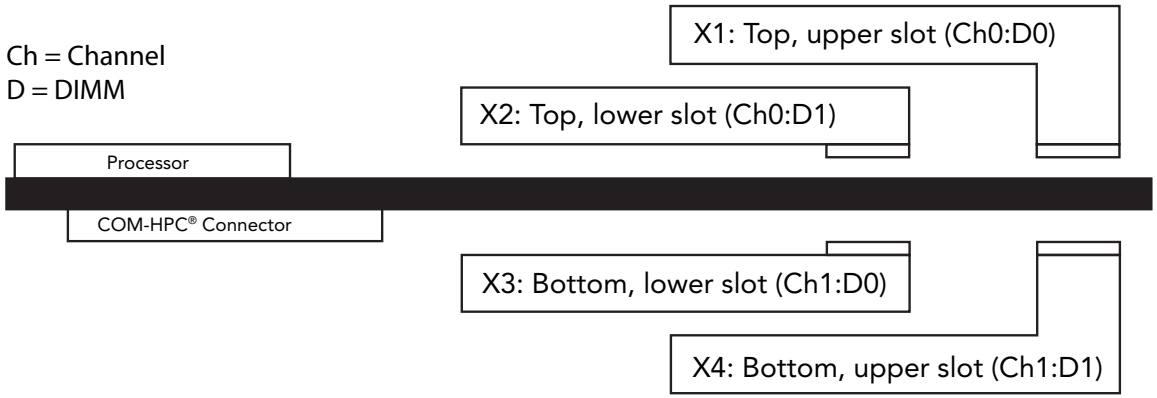
Table 14 Wake Events

Wake Event	Conditions/Remarks
Power Button	Wakes unconditionally from S3-S5
Onboard LAN Event	Device driver must be configured for Wake On LAN support
SMB_ALERT#	Wakes unconditionally from S3-S5; S5e
PCI Express WAKE#	Wakes unconditionally from S3-S5
WAKE#	Wakes unconditionally from S3
PME#	Activate the wake up capabilities of a PCI device using Windows device manager configuration options for this device or set "Resume On PME#" to "Enabled" in the power setup menu
USB Mouse/Keyboard Event	When "Standby mode" is set to S3, USB hardware must be powered by standby power source. Set "USB Device Wakeup" from S3/S4 to "Enabled" in the ACPI setup menu (if setup node is available in BIOS setup program) In device manager, look for the keyboard/mouse devices. Go to the power management tab and check "Allow this device to bring the computer out of standby".
RTC Alarm	Activate and configure "Resume On RTC Alarm" in the power setup menu (only available in S5)
Watchdog Power Button Event	Wakes unconditionally from S3-S5

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8.6 Memory Population Rules

The diagram below shows the location of the four SO-DIMM connectors (X1, X2, X3, and X4) on standard conga-HPC/cBLS module variants:



The following population rules must be observed:

- Either X1 or X4 must be populated or the system will not boot (POST code 55)
- All populated memory modules should have the same part number for optimal performance and to avoid potential issues
- Do not mix ECC and non-ECC memory modules

Note

1. *When populating single-rank (1R) memory modules, the BIOS automatically sets the speed to 4000 MT/s.*
2. *When populating one dual-rank (2R) memory module, the BIOS automatically sets the speed to 3600 MT/s.*
3. *When populating more than one dual-rank (2R) memory module, the BIOS automatically sets the speed to 3200 MT/s.*

Caution

The standard conga-HPC/cBLS module's bottom-side SO-DIMM connectors exceed COM-HPC® height limitations. This design allows for increased system memory capacity but requires special carrier board design considerations:

- *Implement the 10 mm COM-HPC® carrier connector height stack option.*
- *Ensure components do not collide with the module's bottom-side SO-DIMM connectors, including during assembly.*

Failure to follow these design considerations may result in damage to the carrier board and module or cause improper fit.

For a COM-HPC® compliant conga-HPC/cBLS module without bottom-side SO-DIMM connectors, contact your congatec sales representative.

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9 Signal Descriptions and Pinout Tables

This section describes the signals found on the conga-HPC/cBLS. The pinout complies with PICMG® COM-HPC®, revision 1.10. The table below describes the terminology used in this section. The PU/PD column indicates if a pull-up or pull-down resistor has been used. If the field entry area in this column for the signal is empty, then no pull-up or pull-down resistor has been implemented by congatec.

The "#" symbol at the end of the signal name indicates that the active or asserted state occurs when the signal is at a low voltage level. When "#" is not present, the signal is asserted when at a high voltage level.

Note

The Signal Description tables do not list internal pull-ups or pull-downs implemented by the chip vendors. Only pull-ups or pull-downs implemented by congatec are listed. For information about the internal pull-ups or pull-downs implemented by the chip vendors, refer to the respective chip's datasheet.

Table 15 Signal Description Terminology

Term	Description
PU	congatec implemented pull-up resistor
PD	congatec implemented pull-down resistor
T	Higher voltage tolerance
I 1.8 VSB	Input 1.8 V tolerant active in standby state
O 1.8 VSB	Output 1.8 V tolerant active in standby state
I/O 1.8 VSB	Bi-directional signal 1.8 V tolerant active in standby state
I 3.3 V	Input 3.3 V tolerant
O 3.3 V	Output 3.3 V signal level
I/O 3.3 V	Bi-directional signal 3.3 V tolerant
I 3.3 VSB	Input 3.3V tolerant active in standby state
O 3.3 VSB	Output 3.3V tolerant active in standby state
I/O 3.3 VSB	Bi-directional signal 3.3 V tolerant active in standby state
I 5 VSB	Input 5 V tolerant active in standby state
OD	Open drain output
V_{OL}	Output low voltage
V_{OH}	Output high voltage
P	Power Input/Output
DDC	Display Data Channel
PCIE	PCI Express®
SATA	Serial ATA
REF	Reference voltage output. May be sourced from a module power plane.
KR	10GBASE-KR compatible signal
PDS	Pull-down strap. A module output pin that is either tied to GND or is not connected. Used to signal module capabilities (pinout type) to the Carrier Board.

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9.1 Connector Signal Descriptions

Table 16 Primary Connector (J1) Pinout

Pin	Row A	Pin	Row B	Pin	Row C	Pin	Row D
A01	VCC	B01	VCC	C01	VCC	D01	VCC
A02	VCC	B02	PWRBTN#	C02	RSTBTN#	D02	VCC
A03	VCC	B03	VCC	C03	VCC	D03	VCC
A04	VCC	B04	THERMTRIP#	C04	CARRIER_HOT#	D04	VCC
A05	VCC	B05	VCC	C05	VCC	D05	VCC
A06	VCC	B06	TAMPER#	C06	VIN_PWROK	D06	VCC
A07	VCC	B07	VCC	C07	VCC	D07	VCC
A08	VCC	B08	SUS_S3#	C08	SUS_S4_S5#	D08	VCC
A09	VCC	B09	VCC	C09	VCC	D09	VCC
A10	GND	B10	WD_STROBE#	C10	GND	D10	WAKE0#
A11	BATLOW#	B11	WD_OUT	C11	FAN_PWMOUT	D11	WAKE1#
A12	PLTRST#	B12	GND	C12	FAN_TACHIN	D12	GND
A13	GND	B13	USB5-	C13	GND	D13	USB1-
A14	USB7-	B14	USB5+	C14	USB3-	D14	USB1+
A15	USB7+	B15	GND	C15	USB3+	D15	GND
A16	GND	B16	USB4-	C16	GND	D16	USB0-
A17	USB6-	B17	USB4+	C17	USB2-	D17	USB0+
A18	USB6+	B18	GND	C18	USB2+	D18	GND
A19	GND	B19	I2S_LRCLK/SNDW_CLK3/HDA_SYNC	C19	GND	D19	DDI0_SDA_AUX-
A20	DDI1_SDA_AUX-	B20	I2S_DOUT/SNDW_DAT3/HDA_SDOUT [3]	C20	SNDW_DMIC_CLK1	D20	DDI0_SCL_AUX+
A21	DDI1_SCL_AUX+	B21	I2S_MCLK/HDA_RST#	C21	SNDW_DMIC_DAT1	D21	GND
A22	GND	B22	I2S_DIN/SNDW_DAT2/HDA_SDIN	C22	GND	D22	DDI0_PAIR0-
A23	DDI1_PAIR0-	B23	I2S_CLK/SNDW_CLK2/HDA_BITCLK	C23	SNDW_DMIC_CLK0	D23	DDI0_PAIR0+
A24	DDI1_PAIR0+	B24	VCC_5V_SBY	C24	SNDW_DMIC_DAT0	D24	GND
A25	GND	B25	USB67_OC#	C25	GND	D25	DDI0_PAIR1-
A26	DDI1_PAIR1-	B26	USB45_OC#	C26	DDI0_DDC_AUX_SEL	D26	DDI0_PAIR1+
A27	DDI1_PAIR1+	B27	USB23_OC#	C27	DDI1_DDC_AUX_SEL	D27	GND
A28	GND	B28	USB01_OC#	C28	DDI0_HPD	D28	DDI0_PAIR2-
A29	DDI1_PAIR2-	B29	SML1_CLK	C29	DDI1_HPD	D29	DDI0_PAIR2+
A30	DDI1_PAIR2+	B30	SML1_DAT	C30	eDP_HPD	D30	GND
A31	GND	B31	PMCALERT#	C31	eDP_VDD_EN	D31	DDI0_PAIR3-
A32	DDI1_PAIR3-	B32	SML0_CLK	C32	eDP_BKLT_EN	D32	DDI0_PAIR3+
A33	DDI1_PAIR3+	B33	SML0_DAT	C33	eDP_BKLTCTL	D33	GND
A34	GND	B34	USB_PD_ALERT#	C34	GND	D34	AC_PRESENT
A35	eDP_AUX-	B35	USB_PD_I2C_CLK	C35	USB1_AUX- [1]	D35	RSVD [1]
A36	eDP_AUX+	B36	USB_PD_I2C_DAT	C36	USB1_AUX+ [1]	D36	GND
A37	GND	B37	USB_RT_ENA	C37	GND	D37	USB1_SSTX0-

A38	eDP_TX0-	B38	USB1_LSRX [2]	C38	USB1_SSRX0-	D38	USB1_SSTX0+
A39	eDP_TX0+	B39	USB1_LSTX [2]	C39	USB1_SSRX0+	D39	GND
A40	GND	B40	USB0_LSRX [2]	C40	GND	D40	USB1_SSTX1-
A41	eDP_TX1-	B41	USB0_LSTX [2]	C41	USB1_SSRX1-	D41	USB1_SSTX1+
A42	eDP_TX1+	B42	GND	C42	USB1_SSRX1+	D42	GND
A43	GND	B43	USB0_AUX- [1]	C43	GND	D43	USB0_SSTX0-
A44	eDP_TX2-	B44	USB0_AUX+ [1]	C44	USB0_SSRX0-	D44	USB0_SSTX0+
A45	eDP_TX2+	B45	LID#	C45	USB0_SSRX0+	D45	GND
A46	GND	B46	SLEEP#	C46	GND	D46	USB0_SSTX1-
A47	eDP_TX3-	B47	VCC_BOOT_SPI (3.3V)	C47	USB0_SSRX1-	D47	USB0_SSTX1+
A48	eDP_TX3+	B48	BOOT_SPI_CS#	C48	USB0_SSRX1+	D48	GND
A49	GND	B49	BSEL0	C49	GND	D49	SATA0_RX-
A50	eSPI_IO0	B50	BSEL1	C50	BOOT_SPI_IO0 [3]	D50	SATA0_RX+
A51	eSPI_IO1	B51	BSEL2	C51	BOOT_SPI_IO1	D51	GND
A52	eSPI_IO2	B52	eSPI_ALERT0#	C52	BOOT_SPI_IO2 [3]	D52	SATA0_TX-
A53	eSPI_IO3	B53	eSPI_ALERT1#	C53	BOOT_SPI_IO3 [3]	D53	SATA0_TX+
A54	eSPI_CLK	B54	eSPI_CS0#	C54	BOOT_SPI_CLK	D54	GND
A55	GND	B55	eSPI_CS1#	C55	GND	D55	SATA1_RX-
A56	PCIe_CLKREQ0_LO#	B56	eSPI_RST#	C56	PCIe_REFCLK0_HI-	D56	SATA1_RX+
A57	PCIe_CLKREQ0_HI#	B57	GND	C57	PCIe_REFCLK0_HI+	D57	GND
A58	GND	B58	PCIe_BMC_RX- [1]	C58	GND	D58	SATA1_TX-
A59	PCIe_BMC_TX- [1]	B59	PCIe_BMC_RX+ [1]	C59	PCIe_REFCLK0_LO-	D59	SATA1_TX+
A60	PCIe_BMC_TX+ [1]	B60	GND	C60	PCIe_REFCLK0_LO+	D60	GND
A61	GND	B61	PCIe08_RX-	C61	GND	D61	PCIe00_TX-
A62	PCIe08_TX-	B62	PCIe08_RX+	C62	PCIe00_RX-	D62	PCIe00_TX+
A63	PCIe08_TX+	B63	GND	C63	PCIe00_RX+	D63	GND
A64	GND	B64	PCIe09_RX-	C64	GND	D64	PCIe01_TX-
A65	PCIe09_TX-	B65	PCIe09_RX+	C65	PCIe01_RX-	D65	PCIe01_TX+
A66	PCIe09_TX+	B66	GND	C66	PCIe01_RX+	D66	GND
A67	GND	B67	PCIe10_RX-	C67	GND	D67	PCIe02_TX-
A68	PCIe10_TX-	B68	PCIe10_RX+	C68	PCIe02_RX-	D68	PCIe02_TX+
A69	PCIe10_TX+	B69	GND	C69	PCIe02_RX+	D69	GND
A70	GND	B70	PCIe11_RX-	C70	GND	D70	PCIe03_TX-
A71	PCIe11_TX-	B71	PCIe11_RX+	C71	PCIe03_RX-	D71	PCIe03_TX+
A72	PCIe11_TX+	B72	GND	C72	PCIe03_RX+	D72	GND
A73	GND	B73	PCIe12_RX-	C73	GND	D73	PCIe04_TX-
A74	PCIe12_TX-	B74	PCIe12_RX+	C74	PCIe04_RX-	D74	PCIe04_TX+
A75	PCIe12_TX+	B75	GND	C75	PCIe04_RX+	D75	GND
A76	GND	B76	PCIe13_RX-	C76	GND	D76	PCIe05_TX-
A77	PCIe13_TX-	B77	PCIe13_RX+	C77	PCIe05_RX-	D77	PCIe05_TX+
A78	PCIe13_TX+	B78	GND	C78	PCIe05_RX+	D78	GND
A79	GND	B79	PCIe14_RX-	C79	GND	D79	PCIe06_TX-

A80	PCIe14_TX-	B80	PCIe14_RX+	C80	PCIe06_RX-	D80	PCIe06_TX+
A81	PCIe14_TX+	B81	GND	C81	PCIe06_RX+	D81	GND
A82	GND	B82	PCIe15_RX-	C82	GND	D82	PCIe07_TX-
A83	PCIe15_TX-	B83	PCIe15_RX+	C83	PCIe07_RX-	D83	PCIe07_TX+
A84	PCIe15_TX+	B84	GND	C84	PCIe07_RX+	D84	GND
A85	GND	B85	TEST#	C85	GND	D85	NBASET0_MDI0-
A86	VCC_RTC	B86	RSMRST_OUT#	C86	SMB_CLK	D86	NBASET0_MDI0+
A87	SUS_CLK	B87	UART1_TX	C87	SMB_DAT	D87	GND
A88	GPIO_00	B88	UART1_RX	C88	SMB_ALERT#	D88	NBASET0_MDI1-
A89	GPIO_01	B89	UART1_RTS#	C89	UART0_TX	D89	NBASET0_MDI1+
A90	GPIO_02	B90	UART1_CTS#	C90	UART0_RX	D90	GND
A91	GPIO_03	B91	IPMB_CLK	C91	UART0_RTS#	D91	NBASET0_MDI2-
A92	GPIO_04	B92	IPMB_DAT	C92	UART0_CTS#	D92	NBASET0_MDI2+
A93	GPIO_05	B93	GP_SPI_MOSI	C93	I2C0_CLK	D93	GND
A94	GPIO_06	B94	GP_SPI_MISO	C94	I2C0_DAT	D94	NBASET0_MDI3-
A95	GPIO_07	B95	GP_SPI_CS0#	C95	I2C0_ALERT#	D95	NBASET0_MDI3+
A96	GPIO_08	B96	GP_SPI_CS1#	C96	I2C1_CLK	D96	GND
A97	GPIO_09	B97	GP_SPI_CS2#	C97	I2C1_DAT	D97	NBASET0_LINK_MAX#
A98	GPIO_10	B98	GP_SPI_CS3#	C98	NBASET0_SDP	D98	NBASET0_LINK_MID#
A99	GPIO_11	B99	GP_SPI_CLK	C99	NBASET0_CTREF [1]	D99	NBASET0_LINK_ACT#
A100	TYPE0	B100	GP_SPI_ALERT#	C100	TYPE1	D100	TYPE2

Note

1. *Not connected*
2. *Not supported*
3. *Boot strap signal*

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Table 17 Secondary Connector (J2) Pinout

Pin	Row E	Pin	Row F	Pin	Row G	Pin	Row H
E1	RAPID_SHUTDOWN [2]	F1	FUSA_STATUS0 [2]	G1	VCC_5V_SBY	H1	GND
E2	GND	F2	FUSA_STATUS1 [2]	G2	GND	H2	USB2_SSTX0-
E3	DDI2_SDA_AUX-	F3	FUSA_ALERT# [1]	G3	USB2_SSRX0-	H3	USB2_SSTX0+
E4	DDI2_SCL_AUX+	F4	FUSA_SPI_CS# [2]	G4	USB2_SSRX0+	H4	GND
E5	GND	F5	FUSA_SPI_CLK [2]	G5	GND	H5	USB2_SSTX1-
E6	DDI2_PAIR0-	F6	FUSA_SPI_MISO [1]	G6	USB2_SSRX1-	H6	USB2_SSTX1+
E7	DDI2_PAIR0+	F7	FUSA_SPI_MOSI [2]	G7	USB2_SSRX1+	H7	GND
E8	GND	F8	FUSA_SPI_ALERT [1]	G8	GND	H8	USB3_SSTX0-
E9	DDI2_PAIR1-	F9	FUSA_VOLTAGE_ERR# [1]	G9	USB3_SSRX0-	H9	USB3_SSTX0+
E10	DDI2_PAIR1+	F10	PROCHOT#	G10	USB3_SSRX0+	H10	GND
E11	GND	F11	CATERR#	G11	GND	H11	USB3_SSTX1-
E12	DDI2_PAIR2-	F12	RSVD [1]	G12	USB3_SSRX1-	H12	USB3_SSTX1+
E13	DDI2_PAIR2+	F13	RSVD [1]	G13	USB3_SSRX1+	H13	GND
E14	GND	F14	RSVD [1]	G14	GND	H14	USB2_AUX- [1]
E15	DDI2_PAIR3-	F15	RSVD [1]	G15	USB3_LSRX [2]	H15	USB2_AUX+ [1]
E16	DDI2_PAIR3+	F16	RSVD [1]	G16	USB3_LSTX [2]	H16	GND
E17	GND	F17	RSVD [1]	G17	USB2_LSRX [2]	H17	USB3_AUX- [1]
E18	DDI2_DDC_AUX_SEL	F18	RSVD [1]	G18	USB2_LSTX [2]	H18	USB3_AUX+ [1]
E19	DDI2_HPD	F19	GND	G19	PEG_LANE_REV#	H19	GND
E20	GND	F20	PCIe32_RX-	G20	GND	H20	PCIe40_TX-
E21	PCIe32_TX-	F21	PCIe32_RX+	G21	PCIe40_RX-	H21	PCIe40_TX+
E22	PCIe32_TX+	F22	GND	G22	PCIe40_RX+	H22	GND
E23	GND	F23	PCIe33_RX-	G23	GND	H23	PCIe41_TX-
E24	PCIe33_TX-	F24	PCIe33_RX+	G24	PCIe41_RX-	H24	PCIe41_TX+
E25	PCIe33_TX+	F25	GND	G25	PCIe41_RX+	H25	GND
E26	GND	F26	PCIe34_RX-	G26	GND	H26	PCIe42_TX-
E27	PCIe34_TX-	F27	PCIe34_RX+	G27	PCIe42_RX-	H27	PCIe42_TX+
E28	PCIe34_TX+	F28	GND	G28	PCIe42_RX+	H28	GND
E29	GND	F29	PCIe35_RX-	G29	GND	H29	PCIe43_TX-
E30	PCIe35_TX-	F30	PCIe35_RX+	G30	PCIe43_RX-	H30	PCIe43_TX+
E31	PCIe35_TX+	F31	GND	G31	PCIe43_RX+	H31	GND
E32	GND	F32	PCIe36_RX-	G32	GND	H32	PCIe44_TX- [1]
E33	PCIe36_TX-	F33	PCIe36_RX+	G33	PCIe44_RX- [1]	H33	PCIe44_TX+ [1]
E34	PCIe36_TX+	F34	GND	G34	PCIe44_RX+ [1]	H34	GND
E35	GND	F35	PCIe37_RX-	G35	GND	H35	PCIe45_TX- [1]
E36	PCIe37_TX-	F36	PCIe37_RX+	G36	PCIe45_RX- [1]	H36	PCIe45_TX+ [1]
E37	PCIe37_TX+	F37	GND	G37	PCIe45_RX+ [1]	H37	GND
E38	GND	F38	PCIe38_RX- [1]	G38	GND	H38	PCIe46_TX- [1]

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E39	PCIe38_TX- [1]	F39	PCIe38_RX+ [1]	G39	PCIe46_RX- [1]	H39	PCIe46_TX+ [1]
E40	PCIe38_TX+ [1]	F40	GND	G40	PCIe46_RX+ [1]	H40	GND
E41	GND	F41	PCIe39_RX- [1]	G41	GND	H41	PCIe47_TX- [1]
E42	PCIe39_TX- [1]	F42	PCIe39_RX+ [1]	G42	PCIe47_RX- [1]	H42	PCIe47_TX+ [1]
E43	PCIe39_TX+ [1]	F43	GND	G43	PCIe47_RX+ [1]	H43	GND
E44	GND	F44	PCIe16_RX-	G44	GND	H44	PCIe24_TX-
E45	PCIe16_TX-	F45	PCIe16_RX+	G45	PCIe24_RX-	H45	PCIe24_TX+
E46	PCIe16_TX+	F46	GND	G46	PCIe24_RX+	H46	GND
E47	GND	F47	PCIe17_RX-	G47	GND	H47	PCIe25_TX-
E48	PCIe17_TX-	F48	PCIe17_RX+	G48	PCIe25_RX-	H48	PCIe25_TX+
E49	PCIe17_TX+	F49	GND	G49	PCIe25_RX+	H49	GND
E50	GND	F50	PCIe18_RX-	G50	GND	H50	PCIe26_TX-
E51	PCIe18_TX-	F51	PCIe18_RX+	G51	PCIe26_RX-	H51	PCIe26_TX+
E52	PCIe18_TX+	F52	GND	G52	PCIe26_RX+	H52	GND
E53	GND	F53	PCIe19_RX-	G53	GND	H53	PCIe27_TX-
E54	PCIe19_TX-	F54	PCIe19_RX+	G54	PCIe27_RX-	H54	PCIe27_TX+
E55	PCIe19_TX+	F55	GND	G55	PCIe27_RX+	H55	GND
E56	GND	F56	PCIe20_RX-	G56	GND	H56	PCIe28_TX-
E57	PCIe20_TX-	F57	PCIe20_RX+	G57	PCIe28_RX-	H57	PCIe28_TX+
E58	PCIe20_TX+	F58	GND	G58	PCIe28_RX+	H58	GND
E59	GND	F59	PCIe21_RX-	G59	GND	H59	PCIe29_TX-
E60	PCIe21_TX-	F60	PCIe21_RX+	G60	PCIe29_RX-	H60	PCIe29_TX+
E61	PCIe21_TX+	F61	GND	G61	PCIe29_RX+	H61	GND
E62	GND	F62	PCIe22_RX-	G62	GND	H62	PCIe30_TX-
E63	PCIe22_TX-	F63	PCIe22_RX+	G63	PCIe30_RX-	H63	PCIe30_TX+
E64	PCIe22_TX+	F64	GND	G64	PCIe30_RX+	H64	GND
E65	GND	F65	PCIe23_RX-	G65	GND	H65	PCIe31_TX-
E66	PCIe23_TX-	F66	PCIe23_RX+	G66	PCIe31_RX-	H66	PCIe31_TX+
E67	PCIe23_TX+	F67	GND	G67	PCIe31_RX+	H67	GND
E68	GND	F68	RSVD [1]	G68	GND	H68	RSVD [1]
E69	RSVD [1]	F69	RSVD [1]	G69	RSVD [1]	H69	RSVD [1]
E70	RSVD [1]	F70	GND	G70	RSVD [1]	H70	GND
E71	RSVD [1]	F71	NBASET1_MDI0-	G71	GND	H71	CSI1_RX0- [1]
E72	RSVD [1]	F72	NBASET1_MDI0+	G72	CSI0_RX0- [1]	H72	CSI1_RX0+ [1]
E73	RSVD [1]	F73	GND	G73	CSI0_RX0+ [1]	H73	GND
E74	RSVD [1]	F74	NBASET1_MDI1-	G74	GND	H74	CSI1_RX1- [1]
E75	RSVD [1]	F75	NBASET1_MDI1+	G75	CSI0_RX1- [1]	H75	CSI1_RX1+ [1]
E76	RSVD [1]	F76	GND	G76	CSI0_RX1+ [1]	H76	GND
E77	RSVD [1]	F77	NBASET1_MDI2-	G77	GND	H77	CSI1_RX2- [1]
E78	NBASET1_CTREF [1]	F78	NBASET1_MDI2+	G78	CSI0_RX2- [1]	H78	CSI1_RX2+ [1]
E79	NBASET1_SDP	F79	GND	G79	CSI0_RX2+ [1]	H79	GND

E80	NBASET1_LINK_MID#	F80	NBASET1_MDI3-	G80	GND	H80	CSI1_RX3- [1]
E81	NBASET1_LINK_ACT#	F81	NBASET1_MDI3+	G81	CSI0_RX3- [1]	H81	CSI1_RX3+ [1]
E82	NBASET1_LINK_MAX#	F82	GND	G82	CSI0_RX3+ [1]	H82	GND
E83	GND	F83	RSVD [1]	G83	GND	H83	CSI1_CLK- [1]
E84	RSVD [1]	F84	RSVD [1]	G84	CSI0_CLK- [1]	H84	CSI1_CLK+ [1]
E85	RSVD [1]	F85	GND	G85	CSI0_CLK+ [1]	H85	GND
E86	GND	F86	ETH0_TX- [1]	G86	GND	H86	CSI1_I2C_CLK [1]
E87	ETH0_RX- [1]	F87	ETH0_TX+ [1]	G87	CSI0_I2C_CLK [1]	H87	CSI1_I2C_DAT [1]
E88	ETH0_RX+ [1]	F88	GND	G88	CSI0_I2C_DAT [1]	H88	CSI1_MCLK [1]
E89	GND	F89	ETH1_TX- [1]	G89	CSI0_MCLK [1]	H89	CSI1_RST# [1]
E90	ETH1_RX- [1]	F90	ETH1_TX+ [1]	G90	CSI0_RST# [1]	H90	CSI1_ENA [1]
E91	ETH1_RX+ [1]	F91	GND	G91	CSI0_ENA [1]	H91	GND
E92	GND	F92	PCIe_REFCLK2-	G92	GND	H92	PCIe_REFCLKIN0- [1]
E93	PCIe_REFCLK1-	F93	PCIe_REFCLK2+	G93	RSVD [1]	H93	PCIe_REFCLKIN0+ [1]
E94	PCIe_REFCLK1+	F94	GND	G94	RSVD [1]	H94	GND
E95	GND	F95	RSVD [1]	G95	GND	H95	PCIe_REFCLKIN1- [1]
E96	PCIe_CLKREQ1#	F96	ETH0-1_PRSNT# [2]	G96	ETH0-1_I2C_CLK [2]	H96	PCIe_REFCLKIN1+ [1]
E97	PCIe_CLKREQ2#	F97	ETH0-1_PHY_RST# [2]	G97	ETH0-1_I2C_DAT [2]	H97	GND
E98	PCIe_CLKREQ_OUT0# [1]	F98	ETH0_SDP [1]	G98	ETH0-1_PHY_INT# [2]	H98	ETH0-1_MDIO_CLK [1]
E99	PCIe_CLKREQ_OUT1# [1]	F99	ETH1_SDP [1]	G99	ETH0-1_INT# [2]	H99	ETH0-1_MDIO_DAT [2]
E100	PCIe_PERST_IN0# [1]	F100	PCIe_PERST_IN1# [1]	G100	PCIe_WAKE_OUT0# [1]	H100	PCIe_WAKE_OUT1# [1]

Note

1. *Not connected*
2. *Not supported*

Table 18 NBASE-T Ethernet Signal Descriptions

<table>
<tr><th>Gigabit Ethernet</th><th>Pin #</th><th>Description</th><th>I/O</th><th>PU/PD</th><th>Comment</th></tr>
<tr><td>NBASET0_MDI0+
NBASET0_MDI0-
NBASET0_MDI1+
NBASET0_MDI1-
NBASET0_MDI2+
NBASET0_MDI2-
NBASET0_MDI3+
NBASET0_MDI3-

NBASET1_MDI0+
NBASET1_MDI0-
NBASET1_MDI1+
NBASET1_MDI1-
NBASET1_MDI2+
NBASET1_MDI2-
NBASET1_MDI3+
NBASET1_MDI3-</td><td>D86
D85
D89
D88
D92
D91
D95
D94

F72
F71
F75
F74
F78
F77
F81
F80</td><td>Media Dependent Interface Differential Pairs 0,1,2,3. The MDI can operate in 10 Gbps, 1 Gbps, 100 Mbps and 10 Mbps modes.
Some pairs are unused in some modes, per the following:

<table><tr><th></th><th>10000BASE-T
1000BASE-T</th><th>100BASE-TX</th><th>10BASE-T</th></tr><tr><td>MDI[0]+/-</td><td>B1_DA+/-</td><td>TX+/-</td><td>TX+/-</td></tr><tr><td>MDI[1]+/-</td><td>B1_DB+/-</td><td>RX+/-</td><td>RX+/-</td></tr><tr><td>MDI[2]+/-</td><td>B1_DC+/-</td><td></td><td></td></tr><tr><td>MDI[3]+/-</td><td>B1_DD+/-</td><td></td><td></td></tr></table></td><td>I/O MDI
3.3 VSB</td><td></td><td></td></tr>
<tr><td>NBASET0_LINK_ACT#
NBASET1_LINK_ACT#</td><td>D99
E81</td><td>NBASE-T Ethernet Controller activity indicator, active low.
20 mA or more current sink capability at V_{OL} of 0.4V max.
20 mA or more current source capability at V_{OH} of 2.4V min.</td><td>O 3.3 VSB</td><td></td><td></td></tr>
<tr><td>NBASET0_LINK_MAX#
NBASET1_LINK_MAX#</td><td>D97
E82</td><td>NBASE-T Ethernet Controller MAX Speed Link indicator, active low. If active, the link is established at the maximum speed that the Ethernet controller is capable of (which may be 10G, 5G, 2.5G etc).
20 mA or more current sink capability at V_{OL} of 0.4V max.
20 mA or more current source capability at V_{OH} of 2.4V min.</td><td>O 3.3 VSB</td><td></td><td></td></tr>
<tr><td>NBASET0_LINK_MID#
NBASET1_LINK_MID#</td><td>D98
E80</td><td>NBASE-T Ethernet Controller MID Speed Link indicator, active low. If active, the link is established but at a speed lower than what the maximum speed that the Ethernet controller is capable of.
20 mA or more current sink capability at V_{OL} of 0.4V max.
20 mA or more current source capability at V_{OH} of 2.4V min.</td><td>O 3.3 VSB</td><td></td><td></td></tr>
<tr><td>NBASET0_CTREF
NBASET1_CTREF</td><td>C99
E78</td><td>Reference voltage for Carrier Board NBASET Ethernet channel 0 magnetics center tap. The reference voltage is determined by the requirements of the Module PHY and may be as low as 0V and as high as 3.3V.

If not needed, these pins may be left open on the Carrier. The reference voltage output shall be current limited on the Module. In the case in which the reference is shorted to ground, the current shall be limited to 250 mA or less.</td><td>REF</td><td></td><td>Not connected</td></tr>
<tr><td>NBASET0_SDP
NBASET1_SDP</td><td>C98
E79</td><td>NBASE-T Ethernet Controller 0 Software-Definable Pin. Can also be used for IEEE1588 support such as a 1pps signal.</td><td>I/O 3.3 VSB</td><td></td><td></td></tr>
</table>

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Table 19 Ethernet KR and KX Signal Descriptions

Signal	Pin #	Description	I/O	PU/PD	Comment
ETH0_TX+ ETH0_TX-	F87 F86	Ethernet KR ports, transmit output differential pairs.	O KR		Not connected
ETH0_RX+ ETH0_RX-	E88 E87	Ethernet KR ports, receive input differential pairs.	I KR		
ETH1_TX+ ETH1_TX-	F90 F89	Ethernet KR ports, transmit output differential pairs.	O KR		Not connected
ETH1_RX+ ETH1_RX-	E91 E90	Ethernet KR ports, receive input differential pairs.	I KR		
ETH0-1_MDIO_DAT	H99	Management Data I/O interface mode data signal for serial data transfers between the MAC and an external PHY for ETHx ports 0 to 1	I/O 3.3 V	PU 2.2 KΩ 3.3 VSB	Not supported
ETH0-1_MDIO_CLK	H98	Clock signal for Management Data I/O interface mode data signal for serial data transfers between the MAC and an external PHY for ETHx ports 0 to 1.	O 3.3 V		Not connected
ETH0-1_INT#	G99	Active low interrupt signal from IO Port expanders for ETH ports 0 to 1.	I 3.3 V	PU 2.2 KΩ 3.3 VSB	Not supported
ETH0-1_PHY_INT#	G98	Active low PHY interrupt signal from ETH ports 0 to 1.	I 3.3 V	PU 2.2 KΩ 3.3 VSB	
ETH0-1_PHY_RST#	F97	Active low output PHY reset signal for ETH ports 0 to 1.	O 3.3 V	PD 0 RΩ	
ETH0-1_I2C_DAT	G97	I2C data signal of the 2-wire management interface used by the Ethernet KR controller to access the management registers of an external SFP Module or to configure the Carrier PHY for ETHx ports 0 to 3 (Server) or 0 to 1 (Client) and for serialized status information (e.g. LED states).	I/O OD 3.3 V	PU 2.2 KΩ 3.3 VSB	
ETH0-1_I2C_CLK	G96	The I2C clock signals associated with ETH0-3 I2C data lines in the row above.	I/O OD 3.3 V	PU 2.2 KΩ 3.3 VSB	
ETH0_SDP ETH1_SDP	F98 F99	Software-Definable Pins. Can also be used for IEEE1588 support such as a PPS signal.	I/O 3.3 V		Not connected
ETH0-1_PRSNT#	F96	Carrier pulls this line to GND if there is Carrier hardware present to support Ethernet KR signaling on ETH0 or ETH1. If only one KR channel is supported, it should be on ETH0.	I 3.3 V	PU 2.2 KΩ 3.3 VSB	Not supported

Note

The conga-HPC/cBLS does not support Ethernet KR and KX interfaces.

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Table 20 SATA Signal Descriptions

Signal	Pin #	Description	I/O	PU/PD	Comment
SATA0_TX+ SATA0_TX-	D53 D52	Serial ATA channel 0, Transmit Output differential pair.	O SATA		Supports Serial ATA specification 3.2
SATA0_RX+ SATA0_RX-	D50 D49	Serial ATA channel 0, Receive Input differential pair.	I SATA		
SATA1_TX+ SATA1_TX-	D59 D58	Serial ATA channel 1, Transmit Output differential pair.	O SATA		Supports Serial ATA specification 3.2
SATA1_RX+ SATA1_RX-	D56 D55	Serial ATA channel 1, Receive Input differential pair.	I SATA		

Table 21 PCI Express Signal Descriptions

Signal	Pin #	Description	I/O	PU/PD	Comment
PCIe00_TX+ PCIe00_TX-	D62 D61	PCI Express Transmit Output Differential Pairs 0	O PCIE		Supports PCIe Gen 3
PCIe00_RX+ PCIe00_RX-	C63 C62	PCI Express Receive Input Differential Pairs 0	I PCIE		
PCIe01_TX+ PCIe01_TX-	D65 D64	PCI Express Transmit Output Differential Pairs 1	O PCIE		Supports PCIe Gen 3
PCIe01_RX+ PCIe01_RX-	C66 C65	PCI Express Receive Input Differential Pairs 1	I PCIE		
PCIe02_TX+ PCIe02_TX-	D68 D67	PCI Express Transmit Output Differential Pairs 2	O PCIE		Supports PCIe Gen 3
PCIe02_RX+ PCIe02_RX-	C69 C68	PCI Express Receive Input Differential Pairs 2	I PCIE		
PCIe03_TX+ PCIe03_TX-	D71 D70	PCI Express Transmit Output Differential Pairs 3	O PCIE		Supports PCIe Gen 3
PCIe03_RX+ PCIe03_RX-	C72 C71	PCI Express Receive Input Differential Pairs 3	I PCIE		
PCIe04_TX+ PCIe04_TX-	D74 D73	PCI Express Transmit Output Differential Pairs 4	O PCIE		Supports PCIe Gen 3
PCIe04_RX+ PCIe04_RX-	C75 C74	PCI Express Receive Input Differential Pairs 4	I PCIE		
PCIe05_TX+ PCIe05_TX-	D77 D76	PCI Express Transmit Output Differential Pairs 5	O PCIE		Supports PCIe Gen 3
PCIe05_RX+ PCIe05_RX-	C78 C77	PCI Express Receive Input Differential Pairs 5	I PCIE		

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PCIe06_TX+ PCIe06_TX-	D80 D79	PCI Express Transmit Output Differential Pairs 6	O PCIE		Supports PCIe Gen 3
PCIe06_RX+ PCIe06_RX-	C81 C80	PCI Express Receive Input Differential Pairs 6	I PCIE		
PCIe07_TX+ PCIe07_TX-	D83 D82	PCI Express Transmit Output Differential Pairs 7	O PCIE		Supports PCIe Gen 3
PCIe07_RX+ PCIe07_RX-	C84 C83	PCI Express Receive Input Differential Pairs 7	I PCIE		
PCIe08_TX+ PCIe08_TX-	A63 A62	PCI Express Transmit Output Differential Pairs 8	O PCIE		PEG Port Supports PCIe Gen 4 (Default x4; Optional: N/A)
PCIe08_RX+ PCIe08_RX-	B62 B61	PCI Express Receive Input Differential Pairs 8	I PCIE		
PCIe09_TX+ PCIe09_TX-	A66 A65	PCI Express Transmit Output Differential Pairs 9	O PCIE		
PCIe09_RX+ PCIe09_RX-	B65 B64	PCI Express Receive Input Differential Pairs 9	I PCIE		
PCIe10_TX+ PCIe10_TX-	A69 A68	PCI Express Transmit Output Differential Pairs 10	O PCIE		
PCIE10_RX+ PCIE10_RX-	B68 B67	PCI Express Receive Input Differential Pairs 10	I PCIE		
PCIE11_TX+ PCIE11_TX-	A72 A71	PCI Express Transmit Output Differential Pairs 11	O PCIE		
PCIE11_RX+ PCIE11_RX-	B71 B70	PCI Express Receive Input Differential Pairs 11	I PCIE		
PCIE12_TX+ PCIE12_TX-	B75 A74	PCI Express Transmit Output Differential Pairs 12	O PCIE		Supports PCIe Gen 4
PCIE12_RX+ PCIE12_RX-	B74 B73	PCI Express Receive Input Differential Pairs 12	I PCIE		
PCIE13_TX+ PCIE13_TX-	A78 A77	PCI Express Transmit Output Differential Pairs 13	O PCIE		Supports PCIe Gen 4
PCIE13_RX+ PCIE13_RX-	B77 B76	PCI Express Receive Input Differential Pairs 13	I PCIE		
PCIE14_TX+ PCIE14_TX-	A81 A80	PCI Express Transmit Output Differential Pairs 14	O PCIE		Supports PCIe Gen 4
PCIE14_RX+ PCIE14_RX-	B80 B79	PCI Express Receive Input Differential Pairs 14	I PCIE		
PCIE15_TX+ PCIE15_TX-	A84 A83	PCI Express Transmit Output Differential Pairs 15	O PCIE		Supports PCIe Gen 4
PCIE15_RX+ PCIE15_RX-	B83 B82	PCI Express Receive Input Differential Pairs 15	I PCIE		
PCIE16_TX+ PCIE16_TX-	E46 E45	PCI Express Transmit Output Differential Pairs 16	O PCIE		PEG Port Supports PCIe Gen 5 PCIe Gen 5 SSDs are not supported[1]
PCIE16_RX+ PCIE16_RX-	F45 F44	PCI Express Receive Input Differential Pairs 16	I PCIE		

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PCIE17_TX+ PCIE17_TX-	E49 E48	PCI Express Transmit Output Differential Pairs 17	O PCIE		PEG Port Supports PCIe Gen 5 PCIe Gen 5 SSDs are not supported[1]
PCIE17_RX+ PCIE17_RX-	F48 F47	PCI Express Receive Input Differential Pairs 17	I PCIE		
PCIE18_TX+ PCIE18_TX-	E52 E51	PCI Express Transmit Output Differential Pairs 18	O PCIE		PEG Port Supports PCIe Gen 5 PCIe Gen 5 SSDs are not supported[1]
PCIE18_RX+ PCIE18_RX-	F51 F50	PCI Express Receive Input Differential Pairs 18	I PCIE		
PCIE19_TX+ PCIE19_TX-	E55 E54	PCI Express Transmit Output Differential Pairs 19	O PCIE		PEG Port Supports PCIe Gen 5 PCIe Gen 5 SSDs are not supported[1]
PCIE19_RX+ PCIE19_RX-	F54 F53	PCI Express Receive Input Differential Pairs 19	I PCIE		
PCIE20_TX+ PCIE20_TX-	E58 E57	PCI Express Transmit Output Differential Pairs 20	O PCIE		PEG Port Supports PCIe Gen 5 PCIe Gen 5 SSDs are not supported[1]
PCIE20_RX+ PCIE20_RX-	F57 F56	PCI Express Receive Input Differential Pairs 20	I PCIE		
PCIE21_TX+ PCIE21_TX-	E61 E60	PCI Express Transmit Output Differential Pairs 21	O PCIE		PEG Port Supports PCIe Gen 5 PCIe Gen 5 SSDs are not supported[1]
PCIE21_RX+ PCIE21_RX-	F60 F59	PCI Express Receive Input Differential Pairs 21	I PCIE		
PCIE22_TX+ PCIE22_TX-	E64 E63	PCI Express Transmit Output Differential Pairs 22	O PCIE		PEG Port Supports PCIe Gen 5 PCIe Gen 5 SSDs are not supported[1]
PCIE22_RX+ PCIE22_RX-	F63 F62	PCI Express Receive Input Differential Pairs 22	I PCIE		
PCIE23_TX+ PCIE23_TX-	E67 E66	PCI Express Transmit Output Differential Pairs 23	O PCIE		PEG Port Supports PCIe Gen 5 PCIe Gen 5 SSDs are not supported[1]
PCIE23_RX+ PCIE23_RX-	F66 F65	PCI Express Receive Input Differential Pairs 23	I PCIE		
PCIE24_TX+ PCIE24_TX-	H45 H44	PCI Express Transmit Output Differential Pairs 24	O PCIE		PEG Port Supports PCIe Gen 5 PCIe Gen 5 SSDs are not supported[1]
PCIE24_RX+ PCIE24_RX-	G46 G45	PCI Express Receive Input Differential Pairs 24	I PCIE		
PCIE25_TX+ PCIE25_TX-	H48 H47	PCI Express Transmit Output Differential Pairs 25	O PCIE		PEG Port Supports PCIe Gen 5 PCIe Gen 5 SSDs are not supported[1]
PCIE25_RX+ PCIE25_RX-	G46 G45	PCI Express Receive Input Differential Pairs 25	I PCIE		
PCIE26_TX+ PCIE26_TX-	H51 H50	PCI Express Transmit Output Differential Pairs 26	O PCIE		PEG Port Supports PCIe Gen 5 PCIe Gen 5 SSDs are not supported[1]
PCIE26_RX+ PCIE26_RX-	G52 G51	PCI Express Receive Input Differential Pairs 26	I PCIE		
PCIE27_TX+ PCIE27_TX-	H54 H53	PCI Express Transmit Output Differential Pairs 27	O PCIE		PEG Port Supports PCIe Gen 5 PCIe Gen 5 SSDs are not supported[1]
PCIE27_RX+ PCIE27_RX-	G55 G54	PCI Express Receive Input Differential Pairs 27	I PCIE		

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PCIE28_TX+ PCIE28_TX-	H57 H56	PCI Express Transmit Output Differential Pairs 28	O PCIE		PEG Port Supports PCIe Gen 5 PCIe Gen 5 SSDs are not supported[1]
PCIE28_RX+ PCIE28_RX-	G58 G57	PCI Express Receive Input Differential Pairs 28	I PCIE		
PCIE29_TX+ PCIE29_TX-	H60 H59	PCI Express Transmit Output Differential Pairs 29	O PCIE		PEG Port Supports PCIe Gen 5 PCIe Gen 5 SSDs are not supported[1]
PCIE29_RX+ PCIE29_RX-	G61 G60	PCI Express Receive Input Differential Pairs 29	I PCIE		
PCIE30_TX+ PCIE30_TX-	H63 H62	PCI Express Transmit Output Differential Pairs 30	O PCIE		PEG Port Supports PCIe Gen 5 PCIe Gen 5 SSDs are not supported[1]
PCIE30_RX+ PCIE30_RX-	G64 G63	PCI Express Receive Input Differential Pairs 30	I PCIE		
PCIE31_TX+ PCIE31_TX-	H66 H65	PCI Express Transmit Output Differential Pairs 31	O PCIE		PEG Port Supports PCIe Gen 5 PCIe Gen 5 SSDs are not supported[1]
PCIE31_RX+ PCIE31_RX-	G67 G66	PCI Express Receive Input Differential Pairs 31	I PCIE		
PCIE32_TX+ PCIE32_TX-	E22 E21	PCI Express Transmit Output Differential Pairs 32	O PCIE		Supports PCIe Gen 4
PCIE32_RX+ PCIE32_RX-	F21 F20	PCI Express Receive Input Differential Pairs 32	I PCIE		
PCIE33_TX+ PCIE33_TX-	E25 E24	PCI Express Transmit Output Differential Pairs 33	O PCIE		Supports PCIe Gen 4
PCIE33_RX+ PCIE33_RX-	F24 F23	PCI Express Receive Input Differential Pairs 33	I PCIE		
PCIE34_TX+ PCIE34_TX-	E28 E27	PCI Express Transmit Output Differential Pairs 34	O PCIE		Supports PCIe Gen 4
PCIE34_RX+ PCIE34_RX-	F27 F26	PCI Express Receive Input Differential Pairs 34	I PCIE		
PCIE35_TX+ PCIE35_TX-	E31 E30	PCI Express Transmit Output Differential Pairs 35	O PCIE		Supports PCIe Gen 4
PCIE35_RX+ PCIE35_RX-	F30 F29	PCI Express Receive Input Differential Pairs 35	I PCIE		
PCIE36_TX+ PCIE36_TX-	E34 E33	PCI Express Transmit Output Differential Pairs 36	O PCIE		Supports PCIe Gen 3
PCIE36_RX+ PCIE36_RX-	F33 F32	PCI Express Receive Input Differential Pairs 36	I PCIE		
PCIE37_TX+ PCIE37_TX-	E37 E36	PCI Express Transmit Output Differential Pairs 37	O PCIE		Supports PCIe Gen 3
PCIE37_RX+ PCIE37_RX-	F36 F35	PCI Express Receive Input Differential Pairs 37	I PCIE		
PCIE38_TX+ PCIE38_TX-	E40 E39	PCI Express Transmit Output Differential Pairs 38	O PCIE		Not connected
PCIE38_RX+ PCIE38_RX-	F39 F38	PCI Express Receive Input Differential Pairs 38	I PCIE		

PCIE39_TX+ PCIE39_TX-	E43 E42	PCI Express Transmit Output Differential Pairs 39	O PCIE		Not connected
PCIE39_RX+ PCIE39_RX-	F42 F41	PCI Express Receive Input Differential Pairs 39	I PCIE		
PCIE40_TX+ PCIE40_TX-	H21 H20	PCI Express Transmit Output Differential Pairs 40	O PCIE		Supports PCIe Gen 3 Not connected on variants with Q670E chipset.
PCIE40_RX+ PCIE40_RX-	G22 G21	PCI Express Receive Input Differential Pairs 40	I PCIE		
PCIE41_TX+ PCIE41_TX-	H24 H23	PCI Express Transmit Output Differential Pairs 41	O PCIE		Supports PCIe Gen 3 Not connected on variants with Q670E chipset.
PCIE41_RX+ PCIE41_RX-	G25 G24	PCI Express Receive Input Differential Pairs 41	I PCIE		
PCIE42_TX+ PCIE42_TX-	H27 H26	PCI Express Transmit Output Differential Pairs 42	O PCIE		Supports PCIe Gen 3 Not connected on variants with Q670E chipset.
PCIE42_RX+ PCIE42_RX-	G28 G27	PCI Express Receive Input Differential Pairs 42	I PCIE		
PCIE43_TX+ PCIE43_TX-	H30 H29	PCI Express Transmit Output Differential Pairs 43	O PCIE		Supports PCIe Gen 3 Not connected on variants with Q670E chipset.
PCIE43_RX+ PCIE43_RX-	G31 G30	PCI Express Receive Input Differential Pairs 43	I PCIE		
PCIE44_TX+ PCIE44_TX-	H33 H32	PCI Express Transmit Output Differential Pairs 44	O PCIE		Not connected
PCIE44_RX+ PCIE44_RX-	G34 G33	PCI Express Receive Input Differential Pairs 44	I PCIE		
PCIE45_TX+ PCIE45_TX-	H36 H35	PCI Express Transmit Output Differential Pairs 45	O PCIE		Not connected
PCIE45_RX+ PCIE45_RX-	G37 G36	PCI Express Receive Input Differential Pairs 45	I PCIE		
PCIE46_TX+ PCIE46_TX-	H39 H38	PCI Express Transmit Output Differential Pairs 46	O PCIE		Not connected
PCIE46_RX+ PCIE46_RX-	G40 G39	PCI Express Receive Input Differential Pairs 46	I PCIE		
PCIE47_TX+ PCIE47_TX-	H42 H41	PCI Express Transmit Output Differential Pairs 47	O PCIE		Not connected
PCIE47_RX+ PCIE47_RX-	G43 G42	PCI Express Receive Input Differential Pairs 47	I PCIE		
PCIE_BMC_TX+ PCIE_BMC_TX-	A60 A59	PCI Express Differential Transmit Pair for Carrier BMC	O PCIE		Not connected
PCIE_BMC_RX+ PCIE_BMC_RX-	B59 B58	PCI Express Differential Receive Pair for Carrier BMC	I PCIE		
PCIe_REFCLK0_LO+ PCIe_REFCLK0_LO-	C60 C59	Reference clock pair for PCIe lanes [0:7], also referred to as PCIe Group 0 Low and for the PCIe_BMC link	O LV_DIFF		
PCIe_REFCLK0_HI+ PCIe_REFCLK0_HI-	C57 C56	Reference clock pair for PCIe lanes [8:15] also referred to as PCIe Group 0 High	O LV_DIFF		

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PCIe_REFCLK1+ PCIe_REFCLK1-	E94 E93	Reference clock pair for PCIe lanes [16:31] also referred to as PCIe Group 1	O LV_DIFF		
PCIe_REFCLK2+ PCIe_REFCLK2-	F93 F92	Reference clock pair for PCIe lanes [32:47] also referred to as PCIe Group 2	O LV_DIFF		
PCIe_CLKREQ0_LO#	A56	PCIe reference clock request signal from Carrier devices for PCIe_REFCLK0_LO clock pair	Bi-Dir OD 3.3V	PU 10 KΩ 3.3 V	
PCIe_CLKREQ0_HI#	A57	PCIe reference clock request signal from Carrier devices for PCIe_REFCLK0_HI clock pair	Bi-Dir OD 3.3V	PU 10 KΩ 3.3 V	
PCIe_CLKREQ1#	E96	PCIe reference clock request signal from Carrier devices for PCIe_REFCLK1 clock pair	Bi-Dir OD 3.3V	PU 10 KΩ 3.3 V	
PCIe_CLKREQ2#	E97	PCIe reference clock request signals from Carrier devices for PCIe_REFCLK2 clock pair	Bi-Dir OD 3.3V	PU 10 KΩ 3.3 V	
PEG_LANE_REV#	G19	PCI Express Graphics lane reversal input strap. Pull low on the Carrier Board to reverse lane order, otherwise leave COM-HPC pin open. Pulled up on Module or Module chipset to chipset specific power rail.	I 3.3V	PU 100 KΩ 3.3 V	
PCI Express Additional Signals to Support Module-based PCIe Targets					
PCIe_REFCLKIN0+ PCIe_REFCLKIN0-	H93 H92	Reference clock inputs allowing Carrier based root to operate with Module based PCIe targets. The Module designer making use of these clocks should terminate them in a way appropriate to that design.	I LV_DIFF 3.3V		Not connected
PCIe_REFCLKIN1+ PCIe_REFCLKIN1-	H96 H95	Reference clock inputs allowing Carrier based root to operate with Module based PCIe targets. The Module designer making use of these clocks should terminate them in a way appropriate to that design.	I LV_DIFF 3.3V		Not connected
PCIe_WAKE_OUT0#	G100	Wake request signal from Module based PCIe Target to an off-Module PCIe Root complex.	OD 3.3VSB		Not connected
PCIe_WAKE_OUT1#	H100	Wake request signal from Module based PCIe Target to an off-Module PCIe Root complex.	OD 3.3VSB		Not connected
PCIe_PERST_IN0#	E100	Reset signals into Module to reset Module PCIe Targets.	I 3.3V		Not connected
PCIe_PERST_IN1#	F100	Reset signals into Module to reset Module PCIe Targets.	I 3.3V		Not connected

Note

1. *This information is based on the SoC Design Guide and has not been tested by congatec.*

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Table 22 USB Signal Descriptions

USB	Pin #	Description	I/O	PU/PD	Comment
USB0+ USB0-	D17 D16	USB 2.0 differential pairs, channels 0 through 7. USB0 may be configured as a USB client or as a host, or both at the Module designer's discretion. All other USB ports, if implemented, shall be host ports. If any SuperSpeed ports are implemented, then they must be supported by a USB 2.0 port, using one of the USB[0:3] ports from this pool. Specific pairings are detailed below.	I/O USB 3.3 VSB		
USB1+ USB1-	D14 D13		I/O USB 3.3 VSB		
USB2+ USB2-	C18 C17		I/O USB 3.3 VSB		
USB3+ USB3-	C15 C14		I/O USB 3.3 VSB		
USB4+ USB4-	B17 B16		I/O USB 3.3 VSB		
USB5+ USB5-	B14 B13		I/O USB 3.3 VSB		
USB6+ USB6-	A18 A17		I/O USB 3.3 VSB		
USB7+ USB7-	A15 A14		I/O USB 3.3 VSB		
USB0_SSTX0+ USB0_SSTX0-	D44 D43	Four sets of SuperSpeed differential pairs, used to realize one USB 3.2 Gen 2 2x2 port 0. Alternatively, USB 3.2 Gen 1 or Gen 2 ports (single TX pair, single RX pair per port) may be implemented using a portion of this interface. This port shall be used in conjunction with the corresponding USB 2.0 port pair (e.g. USB0 USB 2.0 differential pairs)	O USB SS		Supports USB 3.2 Gen 2 x 2
USB0_SSRX0+ USB0_SSRX0-	C45 C44		I USB SS		
USB0_SSTX1+ USB0_SSTX1-	D47 D46		O USB SS		
USB0_SSRX1+ USB0_SSRX1-	C48 C47		I USB SS		
USB1_SSTX0+ USB1_SSTX0-	D38 D37	Four sets of SuperSpeed differential pairs, used to realize one USB 3.2 Gen 2 2x2 port 1. Alternatively, USB 3.2 Gen 1 or Gen 2 ports (single TX pair, single RX pair per port) may be implemented using a portion of this interface. This port shall be used in conjunction with the corresponding USB 2.0 port pair (e.g. USB1 USB 2.0 differential pairs)	O USB SS		Supports USB 3.2 Gen 2 x 2
USB1_SSRX0+ USB1_SSRX0-	C39 C38		I USB SS		
USB1_SSTX1+ USB1_SSTX1-	D41 D40		O USB SS		
USB1_SSRX1+ USB1_SSRX1-	C42 C41		I USB SS		

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USB2_SSTX0+ USB2_SSTX0-	H03 H02	Four sets of SuperSpeed differential pairs, used to realize one USB 3.2 Gen 2 2x2 port 2. Alternatively, USB 3.2 Gen 1 or Gen 2 ports (single TX pair, single RX pair per port) may be implemented using a portion of this interface. This port shall be used in conjunction with the corresponding USB 2.0 port pair (e.g. USB2 USB 2.0 differential pairs)	O USB SS		Supports USB 3.2 Gen 2 x 2
USB2_SSRX0+ USB2_SSRX0-	G04 G03		I USB SS		
USB2_SSTX1+ USB2_SSTX1-	H06 H05		O USB SS		
USB2_SSRX1+ USB2_SSRX1-	G07 G06		I USB SS		
USB3_SSTX0+ USB3_SSTX0-	H09 H08	Four sets of SuperSpeed differential pairs, used to realize one USB 3.2 Gen 2 2x2 port 3. Alternatively, USB 3.2 Gen 1 or Gen 2 ports (single TX pair, single RX pair per port) may be implemented using a portion of this interface. This port shall be used in conjunction with the corresponding USB 2.0 port pair (e.g. USB3 USB 2.0 differential pairs)	O USB SS		Supports USB 3.2 Gen 2 x 2
USB3_SSRX0+ USB3_SSRX0-	G10 G09		I USB SS		
USB3_SSTX1+ USB3_SSTX1-	H12 H11		O USB SS		
USB3_SSRX1+ USB3_SSRX1-	G13 G12		I USB SS		
USB01_OC#	B28	USB over-current sense, USB channels 0,1; channels 2,3; channels 4,5 and channels 6,7 respectively. A pull-up for each of these lines to the 3.3V Suspend rail shall be present on the Module. The pull-up should be 10K. An open drain driver from USB current monitors on the Carrier Board may drive this line low. The Carrier Board shall not pull these lines up. Note that the over-current limits for USB 2.0 and USB 3.0 are different; this is a Carrier board implementation item.	I 3.3VSB	PU 10 KΩ 3.3 VSB	
USB23_OC#	B27			PU 10 KΩ 3.3 VSB	
USB45_OC#	B26			PU 10 KΩ 3.3 VSB	
USB67_OC#	B25			PU 10 KΩ 3.3 VSB	
RSMRST_OUT#	B86	USB devices that are to be powered in the S5 / S4 / S3 Suspend states should not have their 5V VBUS power enabled before RSMRST_OUT# transitions to the high state.	O 3.3 VSB	PD 100 KΩ	

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Table 23 USB4 Signal Descriptions

Signal	Pin #	Description	I/O	PU/PD	Comment
USB0_AUX+ USB0_AUX-	B44 B43	DisplayPort Aux channel for USB4® DP modes High speed differential pair	LV_DIFF		Not connected
USB1_AUX+ USB1_AUX-	C36 C35	DisplayPort Aux channel for USB4® DP modes High speed differential pair	LV_DIFF		Not connected
USB2_AUX+ USB2_AUX-	H15 H14	DisplayPort Aux channel for USB4® DP modes High speed differential pair	LV_DIFF		Not connected
USB3_AUX+ USB3_AUX-	H18 H17	DisplayPort Aux channel for USB4® DP modes High speed differential pair	LV_DIFF		Not connected
USB0_LSTX	B41	Sideband TX interface for USB4® Alternate modes "Low Speed" asynchronous serial TX line	O 3.3 V	PD 1 MΩ	Not supported
USB0_LSRX	B40	Sideband RX interface for USB4® Alternate modes "Low Speed" asynchronous serial RX line	I 3.3 V	PD 1 MΩ	
USB1_LSTX	B39	Sideband TX interface for USB4 Alternate modes "Low Speed" asynchronous serial TX line	O 3.3 V	PD 1 MΩ	Not supported
USB1_LSRX	B38	Sideband RX interface for USB4® Alternate modes "Low Speed" asynchronous serial RX line	I 3.3 V	PD 1 MΩ	
USB2_LSTX	G18	Sideband TX interface for USB4® Alternate modes "Low Speed" asynchronous serial TX line	O 3.3 V	PD 1 MΩ	Not supported
USB2_LSRX	G17	Sideband RX interface for USB4® Alternate modes "Low Speed" asynchronous serial RX line	I 3.3 V	PD 1 MΩ	
USB3_LSTX	G16	Sideband TX interface for USB4® Alternate modes "Low Speed" asynchronous serial TX line	O 3.3 V	PD 1 MΩ	Not supported
USB3_LSRX	G15	Sideband RX interface for USB4® Alternate modes "Low Speed" asynchronous serial RX line	I 3.3 V	PD 1 MΩ	
SML0_DAT	B33	Data line for I2C data based System Management Links between chipset masters and Carrier. SML0 is used to control the Carrier based USB re-timers and	Bi-Dir OD 3.3 VSB	PU 2.2 KΩ 3.3 VSB	
SML1_DAT	B30	Data line for I2C data based System Management Links between chipset masters and Carrier. SML1 controls the Carrier based USB Power Delivery Controller.	Bi-Dir OD 3.3 VSB	PU 1 KΩ 3.3 VSB	
SML0_CLK	B32	Clock line for System Management Link 0. SML0 is used to support Carrier USB4® Re-Timers	Bi-Dir OD 3.3 V	PU 2.2 KΩ 3.3 VSB	
SML1_CLK	B29	Clock line for System Management Link 1. SML1 is used to support Carrier USB Power Delivery (PD) Controller.	Bi-Dir OD 3.3 V	PU 1 KΩ 3.3 VSB	
PMCALERT#	B31	Active low alert signal associated with the SML1 System Management link, from the Carrier based USB Power Delivery Controller.	I 3.3 V	PU 10 KΩ 3.3 VSB	

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USB_RT_ENA	B37	Power Enable for Carrier based USB Retimers. Sourced from chipset GPO. "USB Re-Timer Enable".	O 3.3 V	PD 100 KΩ	
USB_PD_I2C_DAT	B36	I2C data line between Module based Embedded Controller master and Carrier based USB Power Delivery Controller slave.	Bi-Dir OD 3.3 VSB	PU 1 KΩ 3.3 VSB	
USB_PD_I2C_CLK	B35	I2C clock line between Module based Embedded Controller master and Carrier based USB Power Delivery Controller slave.	Bi-Dir OD 3.3 VSB	PU 1 KΩ 3.3 VSB	
USB_PD_ALERT#	B34	Active low Alert signal from USB Power Delivery Controller to the Module Embedded Controller.	I 3.3 VSB	PU 100 KΩ 3.3 VSB	
Additional Signals to Support USB4® Implementation					
PLTRST#	A12	Platform Reset: output from Module to Carrier Board. Active low. Issued by Module chipset and may result from a low RSTBTN# input, a low VIN_PWR_OK input, a VCC power input that falls below the minimum specification, a watchdog timeout, or may be initiated by the Module software. PLTRST# should remain asserted (low) while the RSTBTN# is low.	O 3.3 VSB	PD 100 KΩ	
SUS_S4_S5#	C08	Indicates system is in Suspend to Disk (S4) or Soft Off (S5) state. Active low output.	O 3.3 VSB	PD 100 KΩ	

Table 24 eSPI Signal Descriptions

Signal	Pin #	Description	I/O	PU/PD	Comment
eSPI_IO0 eSPI_IO1 eSPI_IO2 eSPI_IO3	A50 A51 A52 A53	eSPI Master Data Input / Outputs. These are bi-directional input/output pins used to transfer data between master and slaves.	I/O 1.8 VSB		
eSPI_CS0#	B54	eSPI Master Chip Select Outputs. A low selects a particular eSPI slave for the transaction. Each of the eSPI slaves is connected to a dedicated Chip Select pin. If an eSPI_CSx# pins is not in use, it shall be either pulled high or actively driven high.	O 1.8 VSB	PU 10 KΩ 1.8 VSB	
eSPI_CS1#	B55		O 1.8 VSB	PU 10 KΩ 1.8 VSB	
eSPI_CLK	A54	eSPI Master Clock Output. This pin provides the reference timing for all the serial input and output operations.	O 1.8 VSB		
eSPI_ALERT0# eSPI_ALERT1#	B52 B53	eSPI pins used by eSPI slave to request service from the eSPI master.	I 1.8 VSB	PU 10 KΩ 1.8 VSB	
eSPI_RST#	B56	eSPI Reset - resets the eSPI interface for both master and slaves. eSPI_RST# is typically driven from the eSPI master to eSPI slaves.	O 1.8 VSB	PD 75 KΩ	

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Table 25 Boot SPI Signal Descriptions

Signal	Pin #	Description	I/O	PU/PD	Comment
BOOT_SPI_CS#	B48	Chip select for Carrier Board SPI If the BOOT_SPI_CS# pin is not in use, it shall be either pulled high or actively driven high.	O VCC_BOOT_SPI	PU 10 KΩ 3.3 VSB	
BOOT_SPI_IO0 [1]	C50	Bidirectional 4 bit data path out of and into a Carrier SPI flash operating in Serial Quad Interface (SQI) mode. If the flash memory device is operating in traditional Serial Peripheral Interface (SPI) mode, then signal BOOT_SPI_IO0 is used for getting serial data into the flash device (referred to as SI or MOSI in SPI Flash data sheets) and signal BOOT_SPI_IO1 is used to get serial data from the flash device (referred to as SO or MISO in flash data sheets)	I/O VCC_BOOT_SPI	PU 4.75 KΩ 3.3 VSB	Boot strap signal (see note below)
BOOT_SPI_IO1	C51				
BOOT_SPI_IO2 [1]	C52			PU 100 KΩ 3.3 VSB	Boot strap signal (see note below)
BOOT_SPI_IO3 [1]	C53			PU 100 KΩ 3.3 VSB	Boot strap signal (see note below)
BOOT_SPI_CLK	C54	Clock from Module chipset to Carrier SPI	O VCC_BOOT_SPI	PD 100K	
VCC_BOOT_SPI	B47	Power supply for Carrier Board SPI – sourced from Module – nominally 1.8 V or 3.3 V. The Module shall provide a minimum of 100 mA on VCC_BOOT_SPI. Carriers shall use less than 100 mA from this power source. VCC_BOOT_SPI shall only be used to power SPI devices on the Carrier Board. The Module vendor may choose what power domains the BOOT_SPI is active in.	Power (Out from Module)		3.3 VSB (active in suspend state)

Note

1. *This signal has a special functionality during the reset process. It may strap some basic important function of the module. For more information refer to section 9.2 "Boot Strap Signals".*

Table 26 BIOS Select Signal Descriptions

Signal	Pin #	Description	I/O	PU/PD	Comment
BSEL2	B51	Boot Select pins. These pins distinguish between an SPI or eSPI BIOS boot and between an on-Module or off-Module BIOS. Pulled up on Module to vendor specific power rail.	I 3.3 VSB	PU 10 KΩ 3.3 VSB	Pulled up to 3.3 VSB (active in suspend state)
BSEL1	B50		I 3.3 VSB	PU 10 KΩ 3.3 VSB	
BSEL0	B49		I 3.3 VSB	PU 10 KΩ 3.3 VSB	

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Table 27 DDI Signal Descriptions

Signal	Pin #	Description	I/O	PU/PD	Comment
DDI0_PAIR0+ DDI0_PAIR0-	D23 D22	Digital Display Interface 0 differential pair 0	O LV_DIFF		
DDI0_PAIR1+ DDI0_PAIR1-	D26 D25	Digital Display Interface 0 differential pair 1	O LV_DIFF		
DDI0_PAIR2+ DDI0_PAIR2-	D29 D28	Digital Display Interface 0 differential pair 2	O LV_DIFF		
DDI0_PAIR3+ DDI0_PAIR3-	D32 D31	Digital Display Interface 0 differential pair 3	O LV_DIFF		
DDI1_PAIR0+ DDI1_PAIR0-	A24 A23	Digital Display Interface 1 differential pair 0	O LV_DIFF		
DDI1_PAIR1+ DDI1_PAIR1-	A27 A26	Digital Display Interface 1 differential pair 1	O LV_DIFF		
DDI1_PAIR2+ DDI1_PAIR2-	A30 A29	Digital Display Interface 1 differential pair 2	O LV_DIFF		
DDI1_PAIR3+ DDI1_PAIR3-	A33 A32	Digital Display Interface 1 differential pair 3	O LV_DIFF		
DDI2_PAIR0+ DDI2_PAIR0-	E07 E06	Digital Display Interface 2 differential pair 0	O LV_DIFF		
DDI2_PAIR1+ DDI2_PAIR1-	E10 E09	Digital Display Interface 2 differential pair 1	O LV_DIFF		
DDI2_PAIR2+ DDI2_PAIR2-	E13 E12	Digital Display Interface 2 differential pair 2	O LV_DIFF		
DDI2_PAIR3+ DDI2_PAIR3-	E16 E15	Digital Display Interface 2 differential pair 3	O LV_DIFF		
DDI0_DDC_AUX_SEL DDI1_DDC_AUX_SEL DDI2_DDC_AUX_SEL	C26 C28 E18	Selects the function of DDI[0:2]_SCL_AUX+ and DDI[0:2]_SDA_AUX-. If this input is unconnected on the Carrier, the AUX pair is used for the DP AUX+/- signals. If pulled or driven high on the Carrier, the AUX pair contains the SCL and SDA Display Data Channel (DDC) signals.	I 3.3 V	PD 1 MΩ	DDC I/O and wires must meet I2C-bus Specification, version 2.1, Section 15 for "Standard-Mode" devices. In practice, a max. low-level input voltage of 500 mV is usually sufficient for the DDC signals.
DDI0_SCL_AUX+ DDI1_SCL_AUX+ DDI2_SCL_AUX+	D20 A21 E04	DP AUX+ function if DDI[0:2]_DDC_AUX_SEL is a no connect or driven to GND on the Carrier.	I/O LV_DIFF	PD 100 KΩ	
		SCL Display Data Channel (DDC) if DDI[0:2]_DDC_AUX_SEL is pulled or driven high on the Carrier.	I/O OD 3.3 V	PU 2.2 KΩ 3.3 V	
DDI0_SDA_AUX- DDI1_SDA_AUX- DDI2_SDA_AUX-	D19 A20 E03	DP AUX- function if DDI[0:2]_DDC_AUX_SEL is no connect.	I/O LV_DIFF	PU 100 KΩ 3.3 V	
		SDA Display Data Channel (DDC) if DDI[0:2]_DDC_AUX_SEL is pulled high.	I/O OD 3.3 V	PU 2.2 KΩ 3.3 V	
DDI0_HPD DDI1_HPD DDI2_HPD	C28 C29 E19	DDI Hot-Plug Detect	I 3.3 V	PD 100 KΩ	

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Table 28 eDP Embedded DisplayPort / MIPI DSI Signal Descriptions

Signal	Pin #	Description	I/O	PU/PD	Comment
eDP_TX0+ eDP_TX0-	A39 A38	eDP / DSI differential data pairs Multiplexed with DSI_TX1+ and DSI_TX1-	O LV_DIFF		
eDP_TX1+ eDP_TX1-	A42 A41	eDP / DSI differential data pairs Multiplexed with DSI_TX2+ and DSI_TX2-	O LV_DIFF		
eDP_TX2+ eDP_TX2-	A45 A44	eDP differential data pair DSI differential clock pair Multiplexed with DSI_CLK+ and DSI_CLK-	O LV_DIFF		
eDP_TX3+ eDP_TX3-	A48 A47	eDP / DSI differential data pairs Multiplexed with DSI_TX3+ and DSI_TX3-	O LV_DIFF		
eDP_AUX+ eDP_AUX-	A36 A35	eDP AUX channel differential pair DSI differential data pair Multiplexed with DSI_TX0+ and DSI_TX0-	I/O PCIE LV_DIFF		
eDP_VDD_EN	C31	eDP / DSI power enable Multiplexed with DSI_VDD_EN	O 3.3 V		
eDP_BKLT_EN	C32	eDP / DSI backlight enable Multiplexed with DSI_BKLT_EN	O 3.3 V		
eDP_BKLT_CTRL	C33	EDP / DSI backlight brightness control Multiplexed with DSI_BKLT_CTRL	O 3.3 V		
eDP_HPD	C30	eDP: Detection of Hot Plug / Unplug and notification of the link layer Multiplexed with DSI_TE DSI: Tearing Effect Input: this is an optional signal from the DSI display (that has it's own display controller and frame buffer) coordinating with the host display controller.	I 3.3 V	PD 100 KΩ	

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Table 29 CSI Signal Descriptions

Signal	Pin #	Description	I/O	PU/PD	Comment
CSI0_RX0+ CSI0_RX0-	G73 G72	CSI0 differential data input pairs 0	I LV_DIFF		Not connected
CSI0_RX1+ CSI0_RX1-	G76 G75	CSI0 differential data input pairs 1	I LV_DIFF		
CSI0_RX2+ CSI0_RX2-	G79 G78	CSI0 differential data input pairs 2	I LV_DIFF		
CSI0_RX3+ CSI0_RX3-	G82 G81	CSI0 differential data input pairs 3	I LV_DIFF		
CSI1_RX0+ CSI1_RX0-	H72 H71	CSI1 differential data input pairs 0	I LV_DIFF		Not connected
CSI1_RX1+ CSI1_RX1-	H75 H74	CSI1 differential data input pairs 1	I LV_DIFF		
CSI1_RX2+ CSI1_RX2-	H78 H77	CSI1 differential data input pairs 2	I LV_DIFF		
CSI1_RX3+ CSI1_RX3-	H81 H80	CSI1 differential data input pairs 3	I LV_DIFF		
CSI0_CLK+ CSI0_CLK-	G85 G84	CSI0 differential clock input pairs	I LV_DIFF		Not connected
CSI1_CLK+ CSI1_CLK-	H84 H83	CSI1 differential clock input pairs	I LV_DIFF		Not connected
CSI0_MCLK CSI1_MCLK	G89 H88	CSI Master Clock outputs for CSI0 and CSI1	O 1.8V		Not connected
CSI0_I2C_DAT	G88	CSI-2 Mode: I2C Data line	I/O OD 1.8 V		Not connected
CSI1_I2C_DAT	H87	CSI-2 Mode: I2C Data line	I/O OD 1.8 V		Not connected
CSI0_I2C_CLK	G87	CSI-2 Mode: I2C Clock line	O OD 1.8 V		Not connected
CSI1_I2C_CLK	H86	CSI-2 Mode: I2C Clock line	O OD 1.8 V		Not connected
CSI0_RST#	G90	Active low Reset signals for CSI port 0	O 1.8 V		Not connected
CSI1_RST#	H89	Active low Reset signals for CSI port1	O 1.8 V		Not connected
CSI0_ENA	G91	Active high Enable signals for CSI port 0	O 1.8 V		Not connected
CSI1_ENA	H90	Active high Enable signals for CSI port 1	O 1.8 V		Not connected

Note

The conga-HPC/cBLS does not support the MIPI Camera Serial Interface (CSI).

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Table 30 Soundwire Audio Signal Descriptions

Signal	Pin #	Description	I/O	PU/PD	Comment
SNDW_DMIC_DAT0	C24	Bi-directional PCM audio data	I/O 1.8 V		
SNDW_DMIC_DAT1	C21	Bi-directional PCM audio data	I/O 1.8 V		
SNDW_DMIC_CLK0	C23	Clock for Soundwire transactions	O 1.8 V		
SNDW_DMIC_CLK1	C20	Clock for Soundwire transactions	O 1.8 V		

Note

The SoundWire® and I2S audio ports are not verified because the respective Intel® drivers are currently not available. For a verified audio interface, we recommend to use HDA.

Table 31 I2S / Soundwire / HDA Audio Signal Descriptions

Signal	Pin #	Description	I/O	PU/PD	Comment
I2S_CLK/ SNDW_CLK2/ HDA_BITCLK	B23	I2S Clock Alternative use as Soundwire 2 clock or Serial data clock generated by the external HDA codec	O 1.8 V		
I2S_DIN/ SNDW_DAT2/ HDA_SDIN	B22	I2S Data In. This pin is an input in I2S mode. Alternative use as bi-directional Soundwire 2 data lane or Serial TDM data input	I/O 1.8 V		
I2S_DOUT/ SNDW_DAT3/ HDA_SDOUT [1]	B20	I2S Data Out. This pin is an input in I2S mode Alternative use as bi-directional Soundwire 2 data lane or Serial TDM data output to the codec	I/O 1.8 V		Boot strap signal (see note below)
I2S_LRCLK/ SNDW_CLK3/ HDA_SYNC	B19	I2S L/R Clock Alternative use as Soundwire 3 clock or Sample-synchronization signal to the codec	O 1.8 V		
I2S_MCLK/ HDA_RST#	B21	I2S Master Clock Alternative use as Reset output to codec; active low	O 1.8 V	PD 100 KΩ	

Note

1. *This signal has a special functionality during the reset process. It may strap some basic important function of the module. For more information refer to section 9.2 "Boot Strap Signals".*

2. *The SoundWire® and I2S audio ports are not verified because the respective Intel® drivers are currently not available. For a verified audio interface, we recommend to use HDA.*

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Table 32 Asynchronous Serial Port Signal Descriptions

Signal	Pin #	Description	I/O	PU/PD	Comment
UART0_TX	C89	Logic level asynchronous serial port transmit signal	O 3.3 V		
UART0_RX	C90	Logic level asynchronous serial port receive signal	I 3.3 VSB	PU 47.5 KΩ 3.3 VSB	
UART0_RTS#	C91	Logic level asynchronous serial port Request to Send signal, active low	O 3.3 V		
UART0_CTS#	C92	Logic level asynchronous serial port Clear to Send input, active low	I 3.3 VSB	PU 47.5 KΩ 3.3 VSB	
UART1_TX	B87	Logic level asynchronous serial port transmit signal	O 3.3 V		
UART1_RX	B88	Logic level asynchronous serial port receive signal	I 3.3 VSB	PU 47.5 KΩ 3.3 VSB	
UART1_RTS#	B89	Logic level asynchronous serial port Request to Send signal, active low	O 3.3 V		
UART1_CTS#	B90	Logic level asynchronous serial port Clear to Send input, active low	I 3.3 VSB	PU 47.5 KΩ 3.3 VSB	

Table 33 I2C Signal Descriptions

Signal	Pin #	Description	I/O	PU/PD	Comment
I2C0_CLK	C93	Clock I/O line for the general purpose I2C0 port	I/O OD 3.3 VSB	PU 4.75 KΩ 3.3 VSB	
I2C0_DAT	C94	Data I/O line for the general purpose I2C0 port	I/O OD 3.3 VSB	PU 4.75 KΩ 3.3 VSB	
I2C0_ALERT#	C95	Alert input / interrupt for I2C0	I 3.3 VSB	PU 4.75 KΩ 3.3 VSB	
I2C1_CLK	C96	Clock I/O line for the general purpose I2C1 port	I/O OD **1.8 VSB**	PU 4.75 KΩ **1.8 VSB**	Not 3.3 VSB!
I2C1_DAT	C97	Data I/O line for the general purpose I2C1 port	I/O OD **1.8 VSB**	PU 4.75 KΩ **1.8 VSB**	Not 3.3 VSB!

Table 34 IPMB Signal Descriptions

Signal	Pin #	Description	I/O	PU/PD	Comment
IPMB_CLK	B91	Clock I/O line for the multi-master IPMB port	I/O OD 3.3 VSB	PU 4.75 KΩ 3.3 VSB	
IPMB_DAT	B92	Data I/O line for the multi-master IPMB port	I/O OD 3.3 VSB	PU 4.75 KΩ 3.3 VSB	

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Table 35 General Purpose SPI Signal Descriptions

Signal	Pin #	Description	I/O	PU/PD	Comment
GP_SPI_MISO	B94	Serial data into the COM-HPC Module from the Carrier GP_SPI device ("Master In Slave Out")	I 3.3 V	PU 10 KΩ 3.3 V	
GP_SPI_MOSI [1]	B93	Serial data from the COM-HPC Module to the Carrier GP_SPI device ("Master Out Slave In")	O 3.3 V		May be a boot strap signal depending on assembly option (see note below)
GP_SPI_CLK	B99	Clock from the Module to Carrier GP_SPI device	O 3.3 V		
GP_SPI_CS0#	B95	GP_SPI chip selects, active low	O 3.3 V	PU 10 KΩ 3.3 V	
GP_SPI_CS1#	B96			PU 10 KΩ 3.3 V	
GP_SPI_CS2#	B97			PU 10 KΩ 3.3 V	Not supported
GP_SPI_CS3#	B98			PU 10 KΩ 3.3 V	Not supported
GP_SPI_ALERT#	B100	Alert (interrupt) from a Carrier GP_SPI device to the Module	I 3.3 V	PU 10 KΩ 3.3 VΩ	

Note

1. *Optionally, this signal can be provided by the SoC instead of the cBC and then has a special functionality during the reset process (assembly option). It may strap some basic important function of the module. For more information refer to section 9.2 "Boot Strap Signals".*

Table 36 Power and System Management Signal Descriptions

Signal	Pin #	Description	I/O	PU/PD	Comment
PWRBTN#	B02	A falling edge creates a power button event. Power button events can be used to bring a system out of S5 soft off and other suspend states, as well as powering the system down (with a sustained low).	I 3.3 VSB	PU 100 KΩ 3.3 VSB	
RSTBTN#	C02	Reset button input. The RSTBTN# may be level sensitive (active low) or may be triggered by the falling edge of the signal. The Module PLTRST# signal (below) should not be released (driven or pulled high) while the RSTBTN# is low. For situations when RSTBTN# is not able to reestablish control of the system, VIN_PWR_OK or a power cycle may be used.	I 3.3 VSB	PU 10 KΩ 3.3 VSB	

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PLTRST#	A12	Platform Reset: output from Module to Carrier Board. Active low. Issued by Module chipset and may result from a low RSTBTN# input, a low VIN_PWR_OK input, a VCC power input that falls below the minimum specification, a watchdog timeout, or may be initiated by the Module software. PLTRST# should remain asserted (low) while the RSTBTN# is low.	O 3.3 VSB	PD 100 KΩ	
VIN_PWR_OK	C06	Power OK from main power supply. A high value indicates that the power is good.	I 3.3 V	PU 100 KΩ 3.3 VSB	
SUS_S3#	B08	Indicates system is in Suspend to RAM state. Active low output. An inverted copy of SUS_S3# on the Carrier Board should be used to enable the non-standby power on a typical ATX supply. Even in single input supply system implementations (AT mode, no standby input), the SUS_S3# Module output should be used to disable any Carrier voltage regulators when SUS_S3# is low, to prevent bleed leakage from Carrier circuits into the Module.	O 3.3 VSB	PD 100 KΩ	
SUS_S4_S5#	C08	Indicates system is in Suspend to Disk (S4) or Soft Off (S5) state. Active low output.	O 3.3 VSB	PD 100 KΩ	
SUS_CLK	A87	32.768 kHz +/- 100 ppm clock used by Carrier peripherals such as M.2 cards in their low power modes.	O 3.3 VSB		
WAKE0#	D10	PCI Express wake up signal.	I/O 3.3 VSB	PU 4.7 KΩ 3.3 VSB	
WAKE1#	D11	General purpose wake up signal. May be used to implement wake- up on PS2 keyboard or mouse activity.	I 3.3 VSB	PU 10 KΩ 3.3 VSB	
BATLOW#	A11	Indicates that external battery is low. This port provides a battery-low signal to the Module for orderly transitioning to power saving or power cut-off ACPI modes.	I 3.3 VSB	PU 10 KΩ 3.3 VSB	
LID#	B45	LID switch. Low active signal used by the ACPI operating system for a LID switch.	I 3.3 VSB	PU 47.5 KΩ 3.3 VSB	
SLEEP#	B46	Sleep button. Low active signal used by the ACPI operating system to bring the system to sleep state or to wake it up again.	I 3.3 VSB	PU 100 KΩ 3.3 VSB	
TAMPER#	B06	Tamper or Intrusion detection line on VCC_RTC power well. Carrier hardware pulls this low on a Tamper event.	I 3.3 VSB	PU 1 MΩ 3.3 VSB	
AC_PRESENT	D34	Driven hard low on Carrier if system AC power is not present	I 3.3 VSB	PU 10 KΩ 3.3 VSB	
RSMRST_OUT#	B86	This is a buffered copy of the internal Module RSMRST# (Resume Reset, active low) signal. The internal Module RSMRST# signal is an input to the chipset or SOC and when it transitions from low to high it indicates that the suspend well power rails are stable. USB devices on the Carrier that are to be active in S5 / S3 / S0 should not have their 5V supply applied before RSMRST_OUT# goes high. RSMRST_OUT# shall be a 3.3V CMOS Module output, active in all power states.	O 3.3 VSB	PD 100 KΩ	

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Table 37 Rapid Shutdown Signal Descriptions

Signal	Pin #	Description	I/O	PU/PD	Comment
RAPID_SHUTDOWN	E01	Trigger for Rapid Shutdown. Must be driven to 5 V though a <= 50 Ω source impedance for ≥ 20 µs. Pull-down / disable on Module if RAPID_SHUTDOWN pin is not asserted.	I 5 VSB	PD 100 KΩ	Not supported

Table 38 Thermal Protection Signal Descriptions

Signal	Pin #	Description	I/O	PU/PD	Comment
CARRIER_HOT#	C04	Input from off-Module temp sensor indicating an over-temp situation.	I 3.3 V	PU 10 KΩ 3.3 V	
THERMTRIP#	B04	Active low output indicating that the CPU has entered thermal shutdown.	O 3.3 V	PD 100 KΩ	

Table 39 SMBus Signal Descriptions

Signal	Pin #	Description	I/O	PU/PD	Comment
SMB_CLK	C86	System Management Bus bidirectional clock line.	I/O OD 3.3 VSB	PU 2.2 KΩ 3.3 VSB	
SMB_DAT	C87	System Management Bus bidirectional data line.	I/O OD 3.3 VSB	PU 2.2 KΩ 3.3 VSB	
SMB_ALERT#	C88	System Management Bus Alert – active low input can be used to generate an SMI# (System Management Interrupt) or to wake the system.	I 3.3 VSB	PU 2.2 KΩ 3.3 VSB	

Table 40 General Purpose Input Output Signal Descriptions

Signal	Pin #	Description	I/O	PU/PD	Comment
GPIO_00	A88	General purpose input / output pins. Upon a hardware reset, these pins should be configured as inputs. As inputs, these pins should be able to generate an interrupt to the Module host.	I/O 3.3 VSB	PU 100 KΩ 3.3 VSB	
GPIO_01	A89				
GPIO_02	A90				
GPIO_03	A91				
GPIO_04	A92				
GPIO_05	A93				
GPIO_06	A94				
GPIO_07	A95				
GPIO_08	A96				
GPIO_09	A97				
GPIO_10	A98				
GPIO_11	A99				

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Table 41 Module Type Definition Signal Description

<table>
<tr><th>Signal</th><th>Pin #</th><th>Description</th><th>I/O</th><th>Comment</th></tr>
<tr><td>TYPE0
TYPE1
TYPE2</td><td>A100
C100
D100</td><td>The TYPE pins indicate to the Carrier Board the Pin-out Type that is implemented on the Module. The pins are tied on the Module to either ground (GND) or are no-connects (NC). These pins shall be pulled up on the Carrier, to Carrier standby voltage rail of 5 V or less. Carrier hardware reads the level on these straps.
<table>
<tr><th></th><th colspan="3">Module Connections</th><th rowspan="2">Meaning</th></tr>
<tr><th>Ref</th><th>TYPE2</th><th>TYPE1</th><th>TYPE0</th></tr>
<tr><td>7</td><td>NC</td><td>NC</td><td>NC</td><td>Reserved</td></tr>
<tr><td>6</td><td>NC</td><td>NC</td><td>GND</td><td>Reserved</td></tr>
<tr><td>5</td><td>NC</td><td>GND</td><td>NC</td><td>Reserved</td></tr>
<tr><td>4</td><td>NC</td><td>GND</td><td>GND</td><td>Server module - Fixed 12 V input</td></tr>
<tr><td>3</td><td>GND</td><td>NC</td><td>NC</td><td>Reserved</td></tr>
<tr><td>2</td><td>GND</td><td>NC</td><td>GND</td><td>Reserved</td></tr>
<tr><td>1</td><td>GND</td><td>GND</td><td>NC</td><td>Client module - Wide range 8 V to 20 V input</td></tr>
<tr><td>0</td><td>GND</td><td>GND</td><td>GND</td><td>Client module - Fixed 12 V input</td></tr>
</table>
The module shall implement all three TYPE[x] pins per the table above.
The carrier board should implement combinatorial logic that monitors the Module TYPE pins and keeps power off (e.g deactivates the ATX PS_ON# signal to an ATX power supply or otherwise deactivates VCC to the COM- HPC Module) if an incompatible Module pin-out type is detected. All three TYPE[x] pins should be monitored by the Carrier. The Carrier Board logic may also implement a fault indicator such as an LED.</td><td>PDS</td><td>The conga-HPC/cBLS is a Ref 0 Type module (Client module - Fixed 12 V input). Therefore, the TYPE2, TYPE1, and TYPE0 pins are connected to GND.</td></tr>
</table>

Table 42 Miscellaneous Signal Descriptions

Signal	Pin #	Description	I/O	PU/PD	Comment
WD_OUT	B11	Output indicating that a watchdog time-out event has occurred. Refer to the COM-HPC® Module Base Specification for details.	O 3.3 V	PD 100 KΩ	
WD_STROBE#	B10	Strobe input to watchdog timer. Periodic strobing prevents the watchdog, if enabled, from timing out.	I 3.3 V	PU 10 KΩ 3.3 V	
FAN_PWMOUT	C11	Fan speed control. Uses the Pulse Width Modulation (PWM) technique to control the fan's RPM.	O OD 3.3 V		
FAN_TACHIN	C12	Fan tachometer input for a fan with a two pulse output.	I OD 3.3 V	PU 47.5 KΩ 3.3 V	
TEST#	B85	Module input to allow vendor specific Module test mode(s). Carrier designers should leave this pin open on the Carrier. Designers involved in the design of specialty Carriers for Module test may pull this line to GND or possibly to a Module specific analog voltage between GND and 3.3 V to select a test mode.	I OD 3.3 VSB	PU 10 KΩ 3.3 VSB	

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RSVD	D35	Reserved pins. These may be assigned functions in future versions of this specification. Reserved pins shall not be connected to anything, and shall not be connected to each other.			Not connected
	E69-E77				
	E84-E85				
	F12-F18				
	F68-F69				
	F83-F84				
	F95				
	G69-G70				
	G93-G94				
	H68-H69				

Table 43 External Power Signal Descriptions

Signal	Pin #	Description	I/O	PU/PD	Comment
VCC	A01-A09	Primary power input: fixed +12 V on the Client Type 0; wide range +8 V to +20 V on the Client Type 1; fixed +12 V on the Server. All available VCC pins on the connector shall be used. Refer to COM-HPC® Module Base Specification for details.			
	B01, B03, B05, B07, B09				
	C01, C03, C05, C07, C09				
	D01-D09				
VCC_5V_SBY	B24	Standby power input: +5.0 V nominal. Only used for standby and suspend functions. May be left unconnected if these functions are not used in the system design. Refer to COM-HPC® Module Base Specification for details.			
	G01				
VCC_RTC	A86	Real-time clock circuit-power input. Nominally +3.0 V. Refer to COM-HPC® Module Base Specification for details.			

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Table 44 Functional Safety (FuSa) Support Signal Descriptions

Signal	Pin #	Description	I/O	PU/PD	Comment
FUSA_STATUS0	F01	Two bit FuSa staus / error indication outputs to Carrier based Safety Controller hardware 00 - power off 01 - no error (OK state) 10 - error state (NOK state) 11 - reset state	O CMOS 3.3 V	PU 10 KΩ 3.3 V	
FUSA_STATUS1	F02		O CMOS 3.3 V	PD 0RΩ	
FUSA_ALERT#	F03	Active low output from the COM-HPC Module that signals the occurrence of a correctable error on the COM-HPC Module; the carrier FuSa Safety Controller should query the status via the FuSa SPI interface	O CMOS 3.3 V		Not connected
FUSA_SPI_CS#	F04	Active low chip select into the COM-HPC Module from the Carrier FuSa Safety Controller SPI Master	I CMOS 3.3 V	PU 10 KΩ 3.3 V	
FUSA_SPI_CLK	F05	Clock into the COM-HPC Module from the Carrier FuSa Safety Controller SPI Master	I CMOS 3.3 V	PU 10 KΩ 3.3 V	
FUSA_SPI_MISO	F06	Serial data into the Carrier FuSa SPI Master from the COM-HPC Module SPI Slave (“Master In Slave Out”)	O CMOS 3.3 V		Not connected
FUSA_SPI_MOSI	F07	Serial data from the Carrier FuSa SPI Master, into the COM-HPC Module SPI Slave (“Master Out Slave In”)	I CMOS 3.3 V	PU 10 KΩ 3.3 V	
FUSA_SPI_ALERT	F08	Active high alert output from the COM-HPC Module to alert the Carrier FuSa Safety Controller that Module FuSa SPI data is available for transfer	O CMOS 3.3 V		Not connected
FUSA_VOLTAGE_ERR#	F09	Active low output indicating an over- or under voltage or over-current condition of the monitored voltage rails of the FuSa relevant module power supply	O CMOS 3.3 V		Not connected
PROCHOT#	F10	Active low output indicating a temperature excursion event on the COM-HPC Module	O CMOS 3.3 V	PD 100KΩ	
CATERR#	F11	Active low output indicating a catastrophic error on the COM-HPC CPU or SOC	O CMOS 3.3 V	PD 100KΩ	
THERMTRIP#	B04	Active low output indicating that the CPU has entered thermal shutdown	O CMOS 3.3 V	PD 100KΩ	

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9.2 Boot Strap Signals

Table 45 Boot Strap Signal Descriptions

Signal	Pin #	Description	I/O	PU/PD	Comment
I2S_DOUT/ SNDW_DAT3/ HDA_SDOUT	B20	I2S Data Out. This pin is an input in I2S mode Alternative use as bi-directional Soundwire 2 data lane or Serial TDM data output to the codec	I/O 1.8 V		
GP_SPI_MOSI	B93	Serial data from the COM-HPC Module to the Carrier GP_SPI device ("Master Out Slave In")	O 3.3 V		Not a boot strap signal by default. Boot strap signal in case of assembly option. See section 6.14 "General Purpose SPI Port" for more information.
BOOT_SPI_IO0	C50	Bidirectional 4 bit data path out of and into a Carrier SPI flash operating in Serial Quad Interface (SQI) mode.	I/O VCC_BOOT_SPI	PU 4.75 KΩ 3.3 VSB	
BOOT_SPI_IO2	C52	Bidirectional 4 bit data path out of and into a Carrier SPI flash operating in Serial Quad Interface (SQI) mode.	I/O VCC_BOOT_SPI	PU 100 KΩ 3.3 VSB	
BOOT_SPI_IO3	C53	Bidirectional 4 bit data path out of and into a Carrier SPI flash operating in Serial Quad Interface (SQI) mode.	I/O VCC_BOOT_SPI	PU 100 KΩ 3.3 VSB	

Note

The signals listed in the table above are used as chipset configuration straps during system reset. In this condition (during reset), the COM-HPC® or chipset internally implemented resistors pull these signals to the correct state.

Caution

No external DC loads or external pull-up or pull-down resistors should change the configuration of the signals listed in the above table. External resistors may override the internal strap states and cause the COM-HPC® module to malfunction and/or cause irreparable damage to the module.

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10 System Resources

10.1 I/O Address Assignment

The I/O address assignment of the conga-HPC/cBLS module is functionally identical with a standard PC/AT.

The BIOS assigns PCI and PCI Express I/O resources from FFF0h downwards. Non PnP/PCI/PCI Express compliant devices must not consume I/O resources in that area.

10.1.1 eSPI Bus

On the conga-HPC/cBLS, the PCI Express Bus acts as the subtractive decoding agent. All I/O cycles that are not positively decoded are forwarded to the PCI Express Bus—not the eSPI Bus. Only specified I/O ranges are forwarded to the eSPI Bus.The eSPI Bus from the chipset is connected to COM-HPC® connector and supports two chipselects (CS0, CS1). CS0 is connected to the embedded board controller for exclusive use. In the congatec Embedded BIOS, the following I/O address ranges are sent to the eSPI Bus CS0:

E00h - EFFh (always used internally by the congatec board controller)

eSPI CS1 does not support external devices by default. Optionally, support can be enabled (Custom BIOS option).

10.2 PCI Configuration Space Map

Bus Number (hex)	Device Number (hex)	Function Number (hex)	Description
00h	00h	00h	HOST and DRAM Controller
00h	01h	00h	PEG10/11
00h	02h	00h	Integrated Graphics Device
00h	06h	00h	PEG60
00h	14h	00h	USB3 xHCI Host Controller
00h	14h	02h	Shared SRAM Controller
00h	15h	00h	I2C Controller
00h [1]	16h	00h	Management Engine (ME) Interface 1
00h	17h	00h	SATA Controller
00h [2]	1Ah	00h	PCI Express Root Port 25
00h [2]	1Ah	02h	PCI Express Root Port 27
00h [2]	1Bh	00h	PCI Express Root Port 21

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00h [2]	1Ch	00h	PCI Express Root Port 1
00h [2]	1Ch	01h	PCI Express Root Port 2
00h [2]	1Ch	02h	PCI Express Root Port 3
00h [2]	1Ch	03h	PCI Express Root Port 4
00h [2]	1Ch	04h	PCI Express Root Port 5
00h [2]	1Dh	00h	PCI Express Root Port 9
00h	1Dh	04h	PCI Express Root Port 13 – GBE 1
00h	1Dh	05h	PCI Express Root Port 14 – GBE 0
00h [2]	1Dh	06h	PCI Express Root Port 15
00h [2]	1Dh	07h	PCI Express Root Port 16
00h	1Fh	00h	PCI to eSPI Bridge
00h	1Fh	03h	Intel® High Definition Audio
00h	1Fh	04h	SMBus Controller
00h	1Fh	05h	SPI Flash Controller
01h [3]	00h	00h	PCIe Device connected to PEG Root Port PCIE16
02h [3]	00h	00h	PCIe Device connected to PEG Root Port PCIE4
03h [3]	00h	00h	PCIe Device inserted in PCI Express Port 25 x2
04h [3]	00h	00h	PCIe Device inserted in PCI Express Port 27 x2
05h [3]	00h	00h	PCIe Device inserted in PCI Express Port 21 x4
06h [3]	00h	00h	PCIe Device inserted in PCI Express Port 1 x1
07h [3]	00h	00h	PCIe Device inserted in PCI Express Port 2 x1
08h [3]	00h	00h	PCIe Device inserted in PCI Express Port 3 x1
09h [3]	00h	00h	PCIe Device inserted in PCI Express Port 4 x1
0Ah [3]	00h	00h	PCIe Device inserted in PCI Express Port 5 x4
0Bh [3]	00h	00h	PCIe Device inserted in PCI Express Port 9 x4
0Ch [3]	00h	00h	Intel Ethernet controller I226 GBE 1
0Dh [3]	00h	00h	Intel Ethernet controller I226 GBE 0

Note

1. *In the standard configuration, the Intel Management Engine (ME) related devices are partly present or not present at all.*

2. *The PCI Express Ports are visible only if a device is attached to the PCI Express Slot on the carrier board.*

3. *The Table represents a case when a Single function PCI/PCIe device is connected to all possible slots on the carrier board. The given bus numbers will change based on actual hardware configuration.*

4. *Internal PCI devices not connected to the conga-HPC/cBLS are not listed.*

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10.3 I²C

The addresses below are reserved for Battery Management solutions. Onboard resources are not connected to the I²C busses.

Table 46 Reserved I2C Bus Addresses

8-bit Device Address	7-bit Device Address	Device	Description
0x14	0x0A	congatec Board Controller	Reserved for battery management
0x16	0x0B	congatec Board Controller	Reserved for battery management

10.4 SMBus

The addresses below are reserved on the SMBus of the conga-HPC/cBLS. The SMBus signals are connected to the Intel® chipset.

Table 47 Reserved SMBus Addresses

8-bit Device Address	7-bit Device Address	Device	Comment
0xA0	0x50	Memory SPD	Reserved only if SM BUS isolation is not set to "Always" Check further devices on DDR5 memory.
0xA2	0x51		
0xA4	0x52		
0xA6	0x53		
0x14	0x0A	congatec Board Controller	Reserved for battery management
0x16	0x0B	congatec Board Controller	Reserved for battery management

Note

Do not use the SMBus for off-board non-system management devices. For more information, contact congatec technical support.

10.5 USB PD Bus

The addresses below are reserved on the USB Power Delivery Bus (USB PD Bus) of the conga-HPC/cBLS.

Table 48 Reserved USB PD Bus Addresses

8-bit Device Address	7-bit Device Address	Device	Description
0x40	0x20	Carrier board Post Code Display	Reserved for carrier board Post Code Display
0x42	0x21		

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11 BIOS Setup Description

The BIOS setup description of the conga-HPC/cBLS can be viewed without having access to the module. However, access to the restricted area of the congatec website is required in order to download the necessary tool (CgMlfViewer) and Menu Layout File (MLF).

The MLF contains the BIOS setup description of a particular BIOS revision. The MLF can be viewed with the CgMlfViewer tool. This tool offers a search function to quickly check for supported BIOS features. It also shows where each feature can be found in the BIOS setup menu.

For more information, refer to https://wiki.congatec.com/wiki/BIOS_Setup_Description_(AN42).

Note

If you do not have access to the restricted area of the congatec website, contact your local congatec sales representative.

11.1 Navigating the BIOS Setup Menu

The BIOS setup menu shows the features and options supported in the congatec BIOS. To access and navigate the BIOS setup menu, press the <DEL> or <F2> key during POST. The right frame displays the key legend. Above the key legend is an area reserved for text messages. These text messages explain the options and the possible impacts when changing the selected option in the left frame.

11.2 BIOS Versions

The BIOS displays the BIOS project name and the revision code during POST, and on the main setup screen. The initial production BIOS for conga-HPC/cBLS is identified as GQRSR1xx, where:

- R is the identifier for a BIOS ROM file,
- 1 is the so called feature number and
- xx is the major and minor revision number.

The binary size is 32 MB.

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11.3 Updating the BIOS

BIOS updates are recommeded to correct platform issues or enhance the feature set of the module. The conga-HPC/cBLS features a congatec/AMI AptioEFI firmware on an onboard flash ROM chip. You can update the firmware with the congatec System Utility. The utility has five versions—UEFI shell, DOS based command line[1], Win32 command line, Win32 GUI, and Linux version.

For more information about "Updating the BIOS" refer to the user's guide for the congatec System Utility: https://wiki.congatec.com/wiki/Congatec_System_Utility_-_CGUTIL.

Note

1. *Deprecated*

Caution

The DOS command line tool is not officially supported by congatec and therefore not recommended for critical tasks such as firmware updates. We recommend to use only the UEFI shell for critical updates.

11.3.1 Update from External Flash

For instructions on how to update the BIOS from external flash, refer to https://wiki.congatec.com/wiki/External_BIOS_Update_(AN07).

11.4 Supported Flash Devices

The conga-HPC/cBLS supports the following flash devices:

- Winbond W25R256JVEIQ (32 MB)
- Winbond W25R256JVEIN (32 MB)

The flash devices can be used on the carrier board to support external BIOS. For more information about external BIOS support, refer to https://wiki.congatec.com/wiki/External_BIOS_Update_(AN07).

Note

For the latest supported flash devices, refer to https://wiki.congatec.com/wiki/Supported_SPI_Flash_Devices_for_BIOS.

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