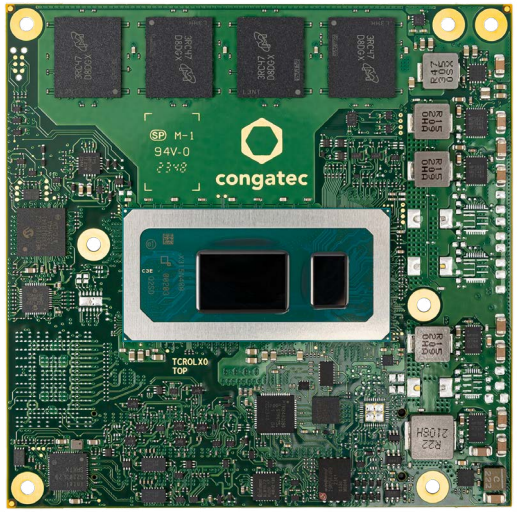

conga-TC675r

COM Express 3.1 Type 6 Compact Module with 13th Generation Intel Processors (Soldered-Down Memory)

User's Guide

Revision 1.00

congatec

Revision History

Revision	Date (yyyy-mm-dd)	Author	Changes
0.01	2024-11-19	KPI	• Preliminary release
0.02	2025-01-28	KPI	• Updated memory description in sections 1.2 “Options Information”, 2.1 “Feature List”, and 3 “Block Diagram” • Updated humidity description in section 2.7 “Environmental Specifications”
1.00	2025-07-21	BEU	• Final release

Preface

This user's guide provides information about the components, features, connectors and system resources available on the conga-TC675r. It is one of three documents that should be referred to when designing a COM Express® application. The other reference documents that should be used include the following:

- COM Express® Module Base Specification
- COM Express® Carrier Design Guide

These documents are available on the PICMG website at **www.picmg.org**. Additionally, check the restricted area of the congatec website at **www.congatec.com** and the website of the respective silicon vendor for relevant documents (Erratum, PCN, Sighting Reports and others).

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Note

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Terminology

Term	Description
CSA	Active Cooling Solution
CSP	Passive Cooling Solution
DSC	Display Stream Compression
DTR	Dynamic Temperature Range
eDP	Embedded DisplayPort
EU	Execution Unit
DDI	Digital Display Interface
GB	Gigabyte
GHz	Gigahertz
HDA	High Definition Audio
HBR	High Bit Rate
HSP	Heatspreader
kB	Kilobyte
kHz	Kilohertz
MB	Megabyte
Mbit	Megabit
MHz	Megahertz
N.A	Not available
N.C	Not connected
PCIe	PCI Express
PCH	Platform Controller Hub
PEG	PCI Express Graphics
SATA	Serial ATA
TBD	To be determined
TCC	Time Coordinated Computing
TDP	Thermal Design Power
TSN	Time Sensitive Networking
UHBR	Ultra High Bit Rate

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1 Introduction

1.1 COM Express® Concept

COM Express® is an open industry standard defined specifically for COMs (computer on modules). Its creation makes it possible to smoothly transition from legacy interfaces to the newest technologies available today. COM Express® modules are available in following form factors:

- Mini 84 mm x 55 mm
- Compact 95 mm x 95 mm
- Basic 125 mm x 95 mm
- Extended 155 mm x 110 mm

Table 1 COM Express® 3.1 Pinout Types

Types	Connector Rows	PCIe Lanes	PEG	SATA Ports	LAN ports	USB 2.0/ SuperSpeed USB	USB4	Display Interfaces
Type 6	A–B C–D	Up to 24	1	Up to 4	1 x NBASE-T	Up to 8 / 4 [1]	2	VGA,LVDS/eDP, PEG, 3x DDI
Type 7	A–B C–D	Up to 32	-	Up to 2	1x NBASE-T, 4x 10GBASE-KR	Up to 4 / 4 [1]	-	
Type 10	A–B	Up to 4	-	Up to 2	1x NBASE-T	Up to 8 / 2 [1]	-	LVDS/eDP, 1x DDI

1. *The SuperSpeed USB ports (USB 3.0) are not in addition to the USB 2.0 ports. Up to 4 of the USB 2.0 ports can support SuperSpeed USB.*

The conga-TC675r modules use the Type 6 pinout definition and comply with COM Express® 3.1 specification. They are equipped with two high performance connectors that ensure stable data throughput.

The COM integrates all the core components and is mounted onto an application specific carrier board. COM modules are legacy-free design (no Super I/O, PS/2 keyboard and mouse) and provide most of the functional requirements for any application. These functions include, but are not limited to a rich complement of contemporary high bandwidth serial interfaces such as PCI Express, Serial ATA, USB 2.0, and Gigabit Ethernet. The robust thermal and mechanical concept, combined with extended power-management capabilities, is perfectly suited for all applications.

Carrier board designers can use as little or as many of the I/O interfaces as deemed necessary. The carrier board can therefore provide all the interface connectors required to attach the system to the application specific peripherals. This versatility allows the designer to create a dense and optimized package, which results in a more reliable product while simplifying system integration.

Most importantly, COM Express® modules are scalable, which means once an application has been created there is the ability to diversify the product range through the use of different performance class or form factor size modules. Simply unplug one module and replace it with another; no redesign is necessary.

1.2 Options Information

The conga-TC675r is currently available in 6 variants. The table below shows the different configurations available.

Table 2 Industrial Variants

Part-No.		045330	045331	045332	045333
Processor		Intel® Core™ i7-13800HRE, 2.5 GHz, 14 Core™	Intel® Core™ i7-1370PRE 1.9 GHz, 14 Core™	Intel® Core™ i7-1365URE 1.7 GHz, 10 Core™	Intel® Core™ i5-13600HRE 2.7 GHz, 12 Core™
Total Core	P-Cores	6 Cores	6 Cores	2 Cores	4 Cores
	E-Cores	8 Cores	8 Cores	8 Cores	8 Cores
No of Threads		20	20	12	16
Core Base Frequency	P-Cores	2.5 GHz	1.9 GHz	1.7 GHz	2.7 GHz
	E-Cores	1.8 GHz	1.2 GHz	1.2 GHz	1.9 GHz
Intel® Smart Cache		24 MB	24 MB	12 MB	18 MB
Base TDP (cTDP down/up)		45 (35/65) W	28 (20/35) W	15 (12/28) W	45 (35/65) W
Maximum Turbo Freq. [1]	P-Cores	5.0 GHz	4.8 GHz	4.9 GHz	4.8 GHz
	E-Cores	4.0 GHz	3.7 GHz	3.7 GHz	3.6 GHz
Processor Graphics		Intel® Iris® Xᵉ Graphics (96 EU)	Intel® Iris® Xᵉ Graphics (96 EU)	Intel® Iris® Xᵉ Graphics (96 EU)	Intel® Iris® Xᵉ Graphics (80 EU)
GFX Max. Dynamic Freq.		1.4 GHz	1.4 GHz	1.3 GHz	1.4 GHz
Onboard LPDDR5x Dual Channel Memory [2]		32 GB Up to 6000 MT/s Non-ECC	16 GB Up to 6400 MT/s Non-ECC	16 GB Up to 6400 MT/s Non-ECC	16 GB Up to 6400 MT/s Non-ECC
PCIe Lanes	Gen 4 (PEG)	1 x8 PEG	1 x4 PEG (default) or 1 x4 SSD (BOM option)	1 x4 PEG (default) or 1 x4 SSD (BOM option)	1 x8 PEG
	Gen 4 (SSD)	1 x4 SSD (BOM option)			1 x4 SSD (BOM option)
	Gen 3	Up to 8 lanes			
Ethernet Controller		Intel® I226-IT	Intel® I226-IT	Intel® I226-IT	Intel® I226-IT
CPU Use Condition [3]		Industrial (Extended Temperature)	Industrial (Extended Temperature)	Industrial (Extended Temperature)	Industrial (Extended Temperature)
CPU Tjunction	Min.	-40°C	-40°C	-40°C	-40°C
	Max.	100°C	100°C	100°C	100°C
DTR (Cold to Hot Transition) [4]		T_{Boot} + 110°C	T_{Boot} + 110°C	T_{Boot} + 110°C	T_{Boot} + 110°C
DTR (Hot to Cold Transition) [4]		T_{Boot} - 110°C	T_{Boot} - 110°C	T_{Boot} - 110°C	T_{Boot} - 110°C
Compatible Carrier Boards		conga-TEVAL/COMe 3.1 evaluation carrier board for COM Express® Type 6 modules conga-TEVAL/COMe 3.0 evaluation carrier board for COM Express® Type 6 modules			

Part-No.		045334	045337
Processor		Intel® Core™ i5-1350PRE 1.8 GHz, 12 Core™	Intel® Core™ i3-1320PRE 1.7 GHz, 8 Core™
Total Core	P-Cores	4 Cores	4 Cores
	E-Cores	8 Cores	4 Cores
No of Threads		12	12
Core Base Frequency	P-Cores	1.8 GHz	1.7 GHz
	E-Cores	1.3 GHz	1.2 GHz
Intel® Smart Cache		12 MB	12 MB
Base TDP (cTDP down/up)		28 (20/35) W	28 (20/35) W
Maximum Turbo Freq. [1]	P-Cores	4.6 GHz	4.6 GHz
	E-Cores	3.4 GHz	3.4 GHz
Processor Graphics		Intel® Iris® Xᵉ Graphics (80 EU)	Intel® UHD Graphics (48 EU)
GFX Max. Dynamic Freq.		1.4 GHz	1.2 GHz
Onboard LPDDR5x Dual Channel Memory [2]		16 GB 6400 MT/s Non-ECC	16 GB 6400 MT/s Non-ECC
PCIe	Gen 4 (PEG)	1 x4 PEG (default) or	1 x4 PEG (default) or
	Gen 4 (SSD)	1 x4 SSD (BOM option)	1 x4 SSD (BOM option)
	Gen 3	Up to 8x lanes	Up to 8x lanes
Ethernet Controller		Intel® I226-IT	Intel® I226-IT
CPU Use Condition [3]		Industrial (Extended Temperature)	Industrial (Extended Temperature)
CPU Tjunction	Min.	-40°C	-40°C
	Max.	100°C	100°C
DTR (Cold to Hot Transition) [4]		T_{Boot} + 110°C	T_{Boot} + 110°C
DTR (Hot to Cold Transition) [4]		T_{Boot} - 110°C	T_{Boot} - 110°C
Compatible Carrier Boards		conga-TEVAL/COMe 3.1 evaluation carrier board for COM Express® Type 6 modules conga-TEVAL/COMe 3.0 evaluation carrier board for COM Express® Type 6 modules	

Note

1. *Disable Turbo mode for industrial use conditions.*
2. *The memory supports In-band ECC.*
3. *Intel SoC use conditions. For more information, see Intel documentation.*
4. *T_{Boot} is the boot temperature. If the Tjunction is not within the DTR range, you must reboot the system. If DTR is at 110°C, the LPDDR5x memory must operate at or below 5200 MT/s. See Intel documentation for more information.*

2 Specifications

2.1 Feature List

Table 3 Feature Summary

Form Factor	COM Express® Compact; Type 6 connector pinout	
CPU	Intel® Core™ 13th Gen Processors Raptor Lake-P (H-Series, P-Series, U-Series)	
DRAM	Up to 32 GB (optional 64 GB) [1] LPDDR5x with up to 6400 MT/s SDRAM [2]; memory down; dual channel; IBECC	
Mass Storage	NVMe x4 SSD (optional) [8]	
Graphics	Intel® UHD Graphics or Intel® Iris® Xe Graphics architecture; up to 96 EUs	
Display	Up to 3x DDI (2x shared with USB4); LVDS or eDP [3]; VGA (optional) [7]	
Ethernet	2.5 GbE with TSN support via Intel® i226 Ethernet controller series	
I/O Interfaces	Up to 8 PCIe Gen4 PEG (H-Series) or up to 4 PCIe Gen4 PEG (P- and U-Series) [4, 8]; up to 8 PCIe Gen3 [5]; up to 2x USB4 (shared with DDI) [6]; 4x USB 3.2 Gen2 (incl. USB 2.0) + 4x USB 2.0; up to 2x SATA; up to 2x UART; CAN (opt.); 8x GPIOs; GP SPI; LPC; SM Bus; I2C	
Audio	HDA	
congatec Board Controller	Multi-Stage Watchdog; non-volatile User Data Storage; Manufacturing and Board Information; Board Statistics I²C bus (fast mode, 400 kHz, multi-master); Power Loss Control; Hardware Health Monitoring; POST Code Redirection	
Embedded BIOS Feature	AMI Aptio® UEFI firmware; 32 Mbyte serial SPI with congatec Embedded BIOS feature; OEM Logo; OEM CMOS default settings; LCD Control; Display Auto Detection; Backlight Control; Flash Update	
Security	Trusted Platform Module (TPM 2.0)	
Power Management	ACPI 6.0 with battery support	
Operating Systems	Microsoft® Windows 11; Microsoft® Windows 11 IoT Enterprise; Microsoft® Windows 10; Microsoft® Windows 10 IoT Enterprise; Linux; Yocto	
Hypervisor	RTS Real-Time Hypervisor	
Temperature Range	Operation -40°C to 85°C	Storage -40°C to 85°C
Humidity	Operation 10% to 85% r. H. non cond.	Storage 5% to 85% r. H. non cond.
Size	95 x 95 mm	

Note

1. *Capacity of 64GB can be supported via BOM option (customized variants).*
2. *LPDDR5 2R 6400 MT/s is currently not supported.*
3. *Both interfaces are not supported at the same time.*
4. *Variants with H-series support 1 x8 PEG port, while variants with P-series and U-series support 1 x4 PEG port.*

5. *PCIe6 is shared with SATA1 and PCIe7 is shared with SATA0.*

6. *DDI1 is shared with USB4 port 1 and DDI2 is shared with USB4 port 2. For USB4 support, a customized BIOS is required.*

7. *For VGA support, you need a customized conga-TC675r variant.*

8. *Variants with P-series and U-series processors support either 1 x4 PEG port or optional NVMe x4 SSD. Both interfaces are not supported at the same time.*

2.2 Supported Operating Systems

The conga-TC675r supports the following operating systems.

- Microsoft® Windows® 10 Enterprise 2021 LTSC
- Microsoft® Windows® 10 IoT Enterprise 2021 LTSC
- Microsoft® Windows® 11 23h2
- Microsoft® Windows® 11 IoT Enterprise 23h2
- Linux Ubuntu (32/64Bit) 22.04.02
- Yocto
- Real Time Systems Hypervisor

Note

1. *The processor supports only 64-bit operating systems.*

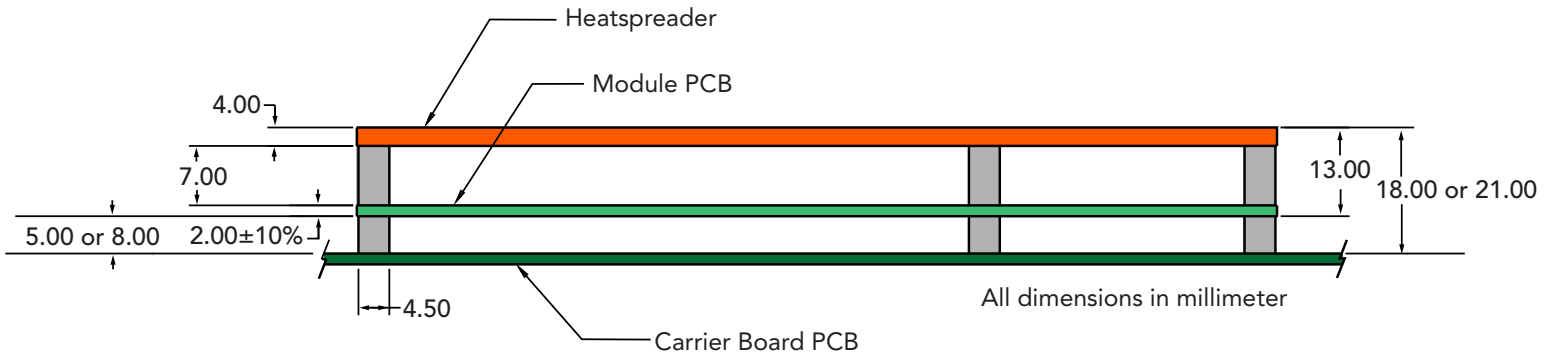
2. *The conga-TC675r supports only native UEFI Operating Systems. Legacy Operating Systems which require CSM (Compatibility Suppport Module) as part of the UEFI firmware are not supported anymore.*

3. *You need kernel 5.15 or higher to support Intel® i226-IT Ethernet controller by default in Linux*

2.3 Mechanical Dimensions

- Length of 95 mm
- Width of 95 mm

The overall height (module, heatspreader and stack) is shown below:



Note

3D models of congatec products are available at www.congatec.com/login These models indicate the overall length, height and width of each product. If you need login access, contact your local sales representative.

2.4 Supply Voltage Standard Power

The conga-TC675r variants **045331, 045332, 045334** and **045337** support a wide input voltage range of **8 V to 20 V** (cTDP up to **35 W**).

The conga-TC675r variants **045330** and **045333** support a wide input voltage range of **11 V to 20 V** (cTDP up to **65 W**).

2.4.1 Electrical Characteristics

Power supply pins on the module's connectors limit the amount of input power. The following table provides an overview of the limitations for pinout Type 6 (dual connector, 440 pins).

Table 4 Overview of Type 6 Limitations

Power Rail	Module Pin Current Capability (Ampere)	Nominal Input (Volts)	Input Range (Volts)	Derated Input (Volts)	Max. Input Ripple (10Hz to 20MHz) (mV)	Max. Module Input Power (w. derated input) (Watts)	Assumed Conversion Efficiency	Max. Load Power (Watts)
VCC_12V	12	12	11.4-12.6	11.4	+/- 100	137	85%	116
VCC_5V-SBY	2	5	4.75-5.25	4.75	+/- 50	9		
VCC_RTC	0.5	3	2.5-3.3		+/- 20			

2.4.2 Rise Time

The input voltages shall rise from 10 percent of nominal to 90 percent of nominal at a minimum slope of 250 V/s. The smooth turn-on requires that, during the 10 percent to 90 percent portion of the rise time, the slope of the turn-on waveform must be positive.

2.5 Power Consumption

The power consumption values were measured with the following setup:

- Input voltage 12 V
- conga-TC675r COM
- Modified congatec carrier board
- conga-TC675r cooling solution
- Microsoft Windows 10 (64 bit)

Note

The CPU was stressed to its maximum workload with the Intel® Power and Thermal Analysis Tool

Table 5 Measurement Description

The power consumption values were recorded during the following system states:

System State	Description	Comment
S0: Minimum value	Lowest frequency mode (LFM) with minimum core voltage during desktop idle	
S0: Maximum value	Highest frequency mode (HFM/Turbo Boost)	The CPU was stressed to its maximum frequency
S0: Peak current	Highest current spike during the measurement of "S0: Maximum value". This state shows the peak value during runtime.	Consider this value when designing the system's power supply to ensure that sufficient power is supplied during worst case scenarios
S3	COM is powered by VCC_5V_SBY	
S5	COM is powered by VCC_5V_SBY	
S5e	COM is powered by VCC_5V_SBY	

Note

1. *The fan and SATA drives were powered externally.*
2. *All other peripherals except the LCD monitor were disconnected before measurement*

The table below provides the TDP Base power current values for the conga-TC675r at various system states:

Table 6 Power Consumption Values

Part No.	Memory Size	H.W Rev.	BIOS Rev.	OS (64 bit)	CPU				Current (Ampere)					
					Variant	P / E Core	Core Freq. P / E (GHz)	Turbo Freq. P / E Core (GHz)	S0: Min	S0: Max	S0: Peak	S3	S5	S5e
045330	4 x 8 GB	A.1	TCROR321	Windows 10	Intel® Core™ i7-13800HRE	6 / 8	2.5 / 1.8	5.0 / 4.0	0.60	10.75	17.98	0.202	0.196	0.0006
045331	2 x 4 GB	A.1	TCROR321	Windows 10	Intel® Core™ i7-1370PRE	6 / 8	1.9 / 1.2	4.8 / 3.7	0.43	4.34	9.93	0.194	0.190	0.0006
045332	4 x 4 GB	A.1	TCROR321	Windows 10	Intel® Core™ i7-1365URE	2 / 8	1.7 / 1.2	4.9 / 3.7	0.39	2.26	7.28	0.200	0.196	0.0006
045333	4 x 4 GB	A.1	TCROR321	Windows 10	Intel® Core™ i5-13600HRE	4 / 8	2.7 / 1.9	4.8 / 3.6	0.48	10.74	14.71	0.200	0.194	0.0006
045334	4 x 4 GB	A.1	TCROR321	Windows 10	Intel® Core™ i5-1350PRE	4 / 8	1.8 / 1.3	4.6 / 3.4	0.39	4.11	8.18	0.200	0.194	0.0006
045337	4 x 4 GB	A.1	TCROR321	Windows 10	Intel® Core™ i3-1320PRE	4 / 4	1.7 / 1.2	4.6 / 3.3	0.51	4.28	7.64	0.216	0.210	0.0006

Note

The power consumption values of other variants are available on request. For more information, contact your local sales representative.

2.6 Supply Voltage Battery Power

Table 7 CMOS Battery Power Consumption

RTC @	Voltage	Current
-50°C	3V DC	2.49 µA
20°C	3V DC	2.71 µA
95°C	3V DC	7.48 µA

Note

1. *Do not use the CMOS battery power consumption values listed above to calculate CMOS battery lifetime.*
2. *Measure the CMOS battery power consumption of your application in worst case conditions (for example, during high temperature and high battery voltage).*
3. *Consider the self-discharge of the battery when calculating the lifetime of the CMOS battery. For more information, refer to application note AN9_RTC_Battery_Lifetime.pdf on congatec GmbH website at www.congatec.com/support/application-notes.*
4. *We recommend to always have a CMOS battery present when operating the conga-TC675r.*

2.7 Environmental Specifications

Temperature (industrial variants)	Operation: -40° to 85°C	Storage: -40° to 85°C
Relative Humidity	10% to 85% r. H. non cond.	Storage: 5% to 85% r. H. non cond.

Caution

The above operating temperatures must be strictly adhered to at all times. When using a congatec heatspreader, the maximum operating temperature refers to any measurable spot on the heatspreader's surface. Humidity specifications are for non-condensing conditions.

2.8 Storage Specifications

This section describes the storage conditions that must be observed for optimal performance of congatec products.

2.8.1 Module

For long-term storage of the conga-TC675r (more than six months), keep the conga-TC675r in a climate-controlled building at a constant temperature between 5°C and 40°C, with humidity of less than 65% and at an altitude of less than 3000 m. Also ensure the storage location is dry and well ventilated.

Note

We do not recommend storing the conga-TC675r for more than five years under these conditions.

2.8.2 Cooling Solution

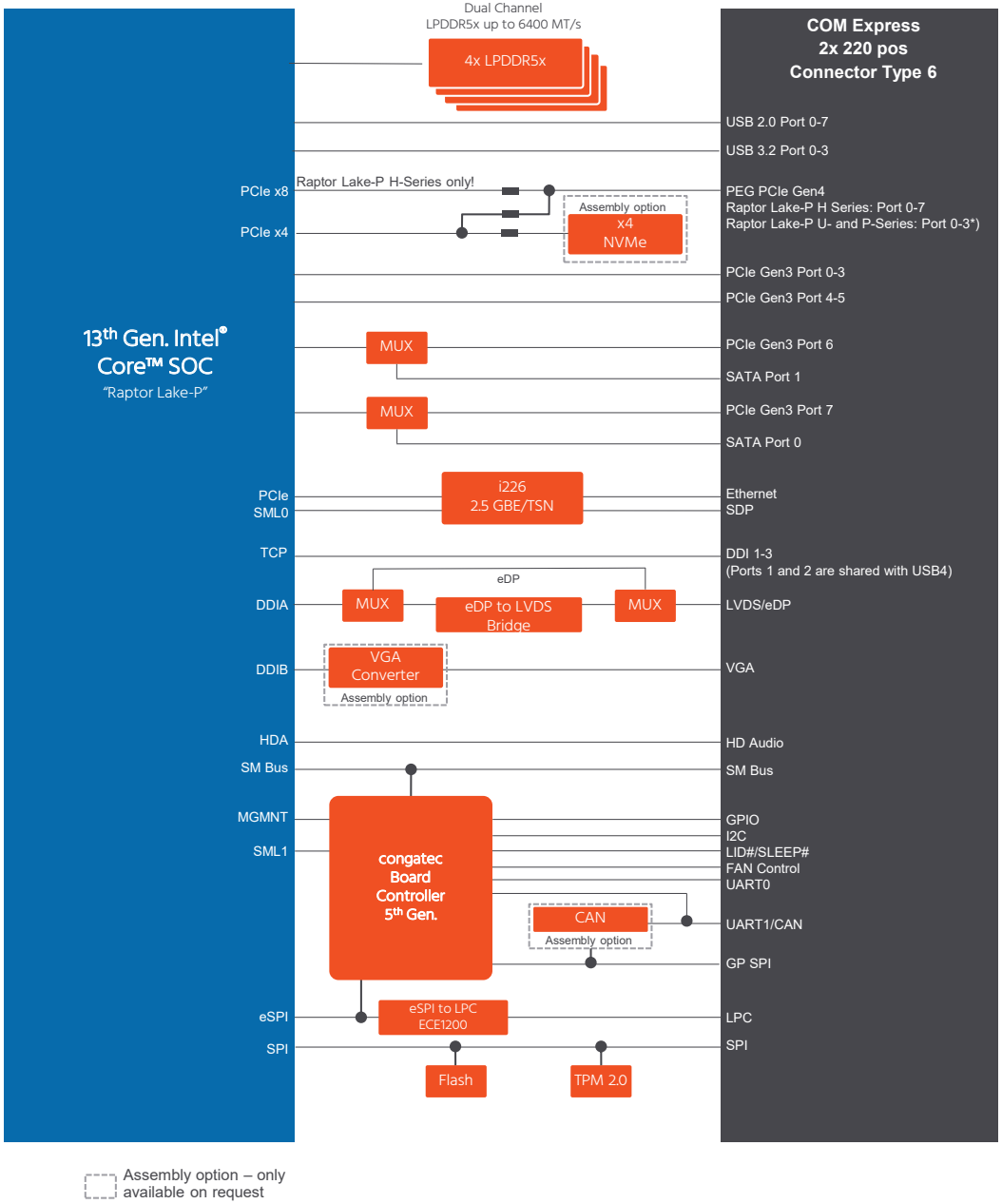
The heatpipes of congatec heatspreaders/cooling solutions are filled with water by default. For optimal cooling performance, do not store the heatspreaders/cooling solutions at temperatures below -20°C.

Caution

1. *For temperatures between -10°C and -20°C, preheat the heatpipes before operation. Optionally, the heatpipes can be filled with acetone instead. For more information, contact your local sales representative.*

2. *For optimal thermal dissipation, do not store the congatec cooling solutions for more than six months.*

3 Block Diagram



*) If Assembly option for NVMe is used there is no PCIe support on PEG Port

4 Cooling Solutions

congatec GmbH offers the following cooling solutions for the conga-TC675r. The dimensions of the cooling solutions are shown in the sub-sections. All measurements are in millimeters.

Table 8 Cooling Solution Variants

	Cooling Solution	Part No	Description
1	CSA	049750	Active cooling solution with integrated heat pipes, 25.5 mm height and 2.7 mm bore-hole standoffs
		049751	Active cooling with integrated heat pipes, 25.5 mm height and M2.5 mm threaded standoffs
2	CSP	049752	Passive cooling solution with integrated heat pipes, 24.7 mm height and 2.7 mm bore-hole standoffs
		049753	Passive cooling solution with integrated heat pipes, 24.7 mm height and M2.5 mm threaded standoffs
3	HSP	049754	Heatspreader with integrated heat pipes, 11 mm height and 2.7 mm bore-hole standoffs
		049755	Heatspreader with with integrated heat pipes, 11 mm height and M2.5 mm threaded standoffs

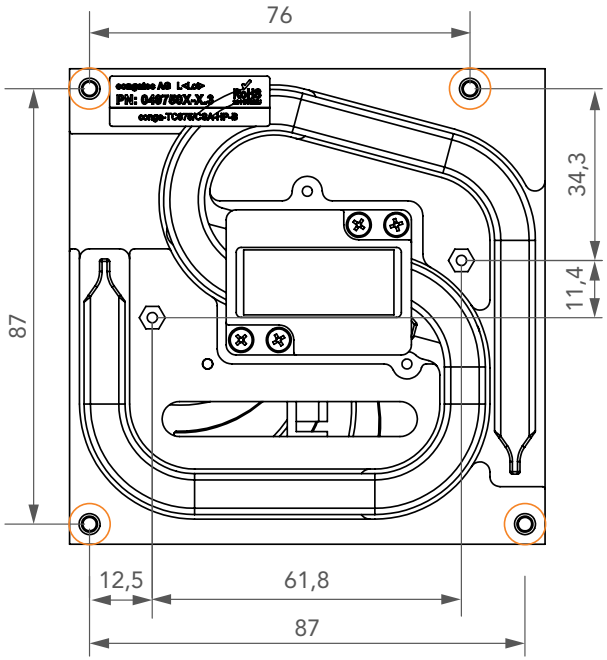
Note

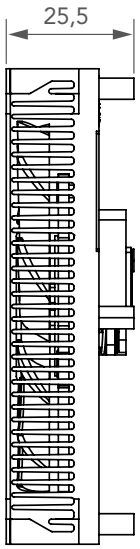
1. *We recommend a maximum torque of 0.4 Nm for carrier board mounting screws and 0.5 Nm for module mounting screws.*
2. *The gap pad material used on congatec heatspreaders may contain silicon oil that can seep out over time depending on the environmental conditions it is subjected to. For more information about this subject, contact your local congatec sales representative and request the gap pad material manufacturer's specification.*
3. *For optimal thermal dissipation, do not store the congatec cooling solutions for more than six months.*

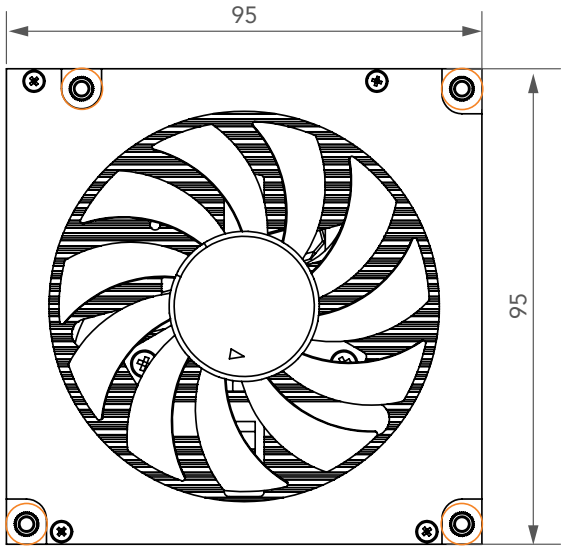
Caution

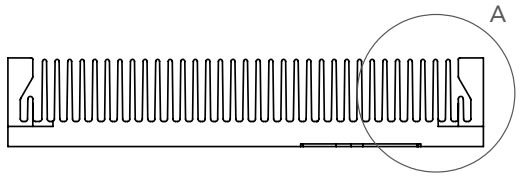
1. *The congatec heatspreaders/cooling solutions are tested only within the commercial temperature range of 0° to 60°C. If your application that features a congatec heatspreader/cooling solution operates outside this temperature range, ensure the correct operating temperature of the module is maintained at all times. This may require additional cooling components for your final application's thermal solution.*
2. *For adequate heat dissipation, use the mounting holes on the cooling solution to attach it to the module. Apply thread-locking fluid on the screws if the cooling solution is used in a high shock and/or vibration environment. To prevent the standoff from stripping or cross-threading, use non-threaded carrier board standoffs to mount threaded cooling solutions.*
3. *For applications that require vertically-mounted cooling solution, use only coolers that secure the thermal stacks with fixing post. Without the fixing post feature, the thermal stacks may move.*
4. *Do not exceed the recommended maximum torque. Doing so may damage the module or the carrier board, or both.*

4.1 CSA Dimensions



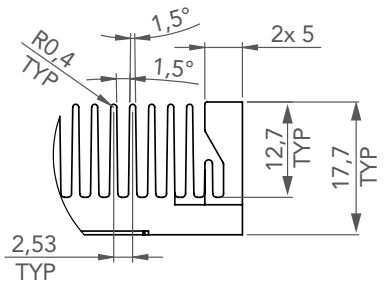


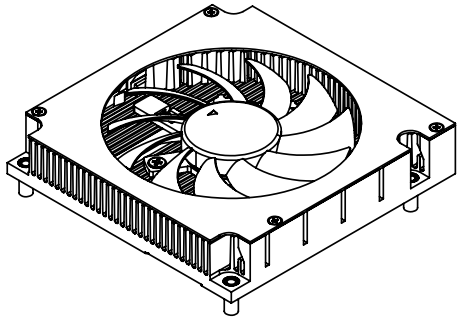


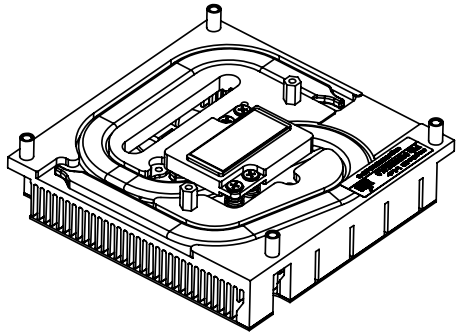


M2.5 x 11 mm
threaded standoff
for threaded version
or
ø2.7 x 11 mm
non-threaded standoff
for borehole version

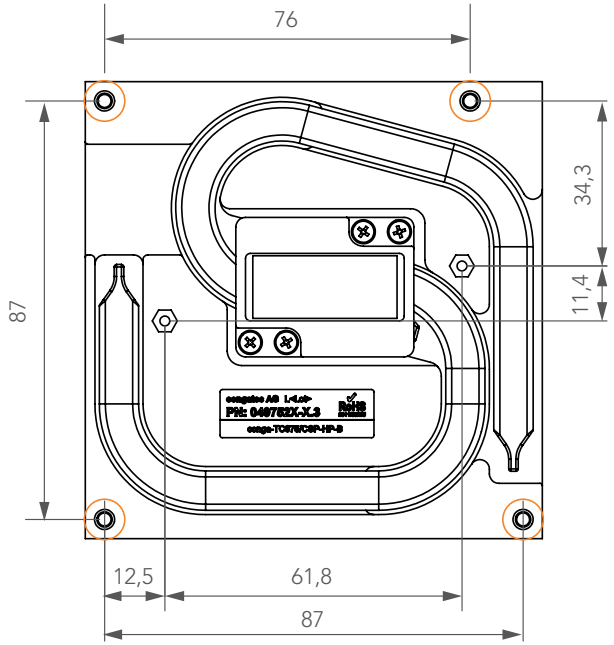
A (3 : 2)

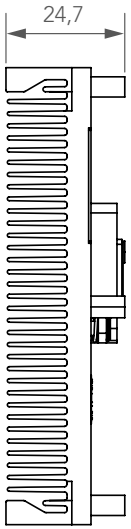


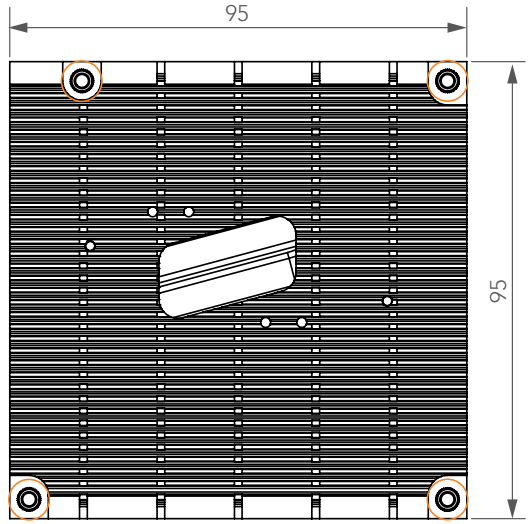


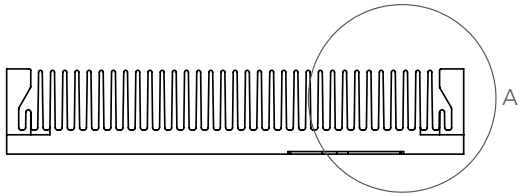


4.2 CSP Dimensions



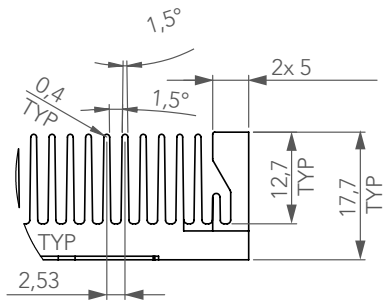


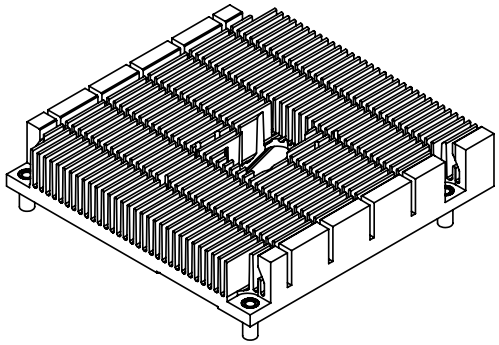


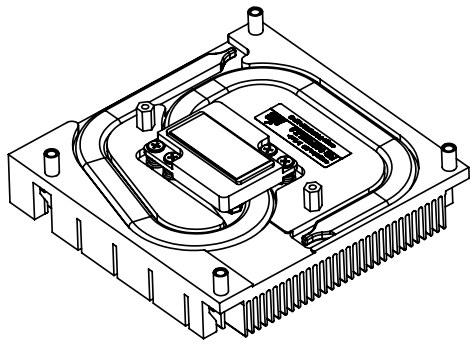


M2.5 x 11 mm
threaded standoff
for threaded version
or
ø2.7 x 11 mm
non-threaded standoff
for borehole version

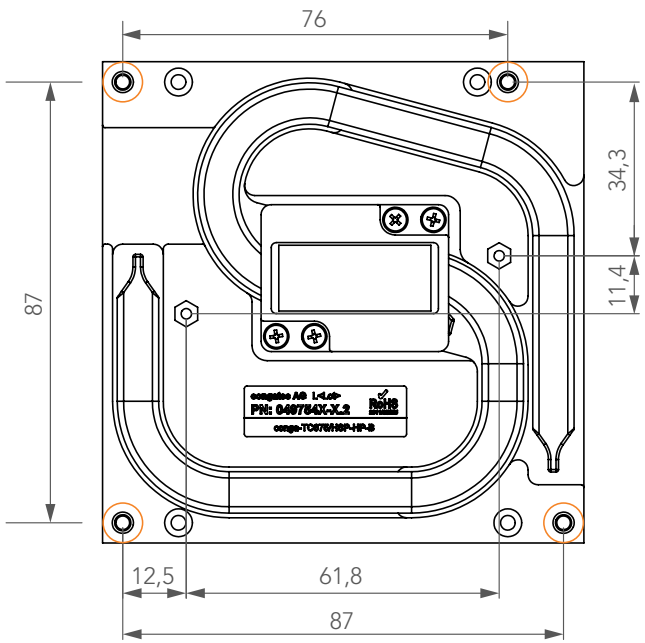
A (3 : 2)

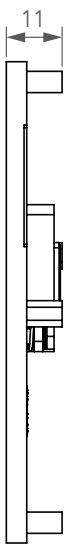


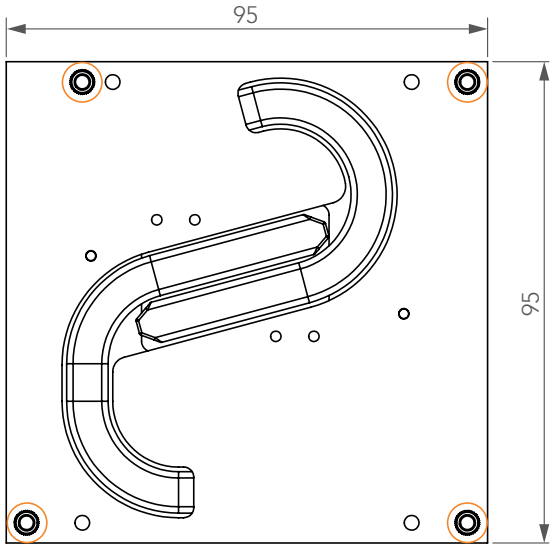




4.3 HSP Dimensions







M2.5 x 11 mm
threaded standoff
for threaded version
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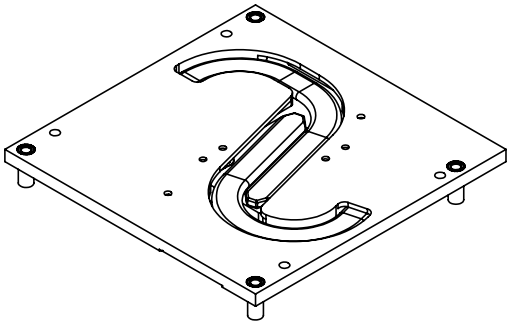
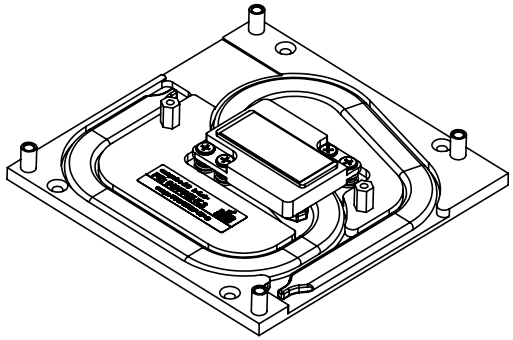
non-threaded standoff
for borehole version





5 Connector Rows

The conga-TC675r is connected to the carrier board via two 220-pin connectors (COM Express® Type 6 pinout). These connectors are broken down into four rows. The primary connector consists of rows A and B while the secondary connector consists of rows C and D.

5.1 PCI Express

The conga-TC675r offers up to eight PCIe lanes – up to six lanes on the A–B connector and up to two lanes (shared with SATA ports) on the C–D connector. The conga-TC675r supports the following:

- up to 8 GTps (Gen 3) speed
- a 6x1 link default configuration (SATA ports are enabled by default) [1, 2, 3]
- lane polarity inversion

Note

1. *PCIe lane 6 and PCIe lane 7 are multiplexed with SATA port 1 and SATA port 0 respectively.*
2. *The multiplexed ports are configurable via the BIOS setup menu.*
3. *The number of PCIe lanes increases if you disable the multiplexed SATA ports.*

Table 9 Default PCIe Link Configuration (with SATA Ports Enabled)

Lanes	PCIe 0	PCIe 1	PCIe 2	PCIe 3	PCIe 4	PCIe 5	PCIe 6	PCIe 7
Link Configuration	x1	x1	x1	x1	x1	x1	N.A	N.A
	x2		x2		x2		N.A	
	x4				N.A			

Note

Maximum of six devices can be enabled.

Table 10 Default PCIe Link Configuration (with SATA Ports Disabled)

Lanes	PCIe 0	PCIe 1	PCIe 2	PCIe 3	PCIe 4	PCIe 5	PCIe 6	PCIe 7
Link Configuration	x1	x1	x1	x1	x1	x1	x1	x1
	x2		x2		x2		x2	
	x4				x4			

Note

Maximum of six devices can be enabled.

5.2 PCI Express Graphics (PEG)

The conga-TC675r supports the following PCIe Gen4 ports on the C–D connector:

- a PCIe x8 Gen 4 (PEG) port on modules that feature the H-series processors [1]
- a PCIe x4 Gen 4 (PEG) port on modules that feature the P-series or the U-series processor [1]

The ports support both graphics [2] and storage devices.

Note

1. *The PEG lanes can not be linked together with the PCI Express lanes in section 5.1 "PCI Express".*
2. *Intel did not validate using the PEG port for graphics on U-series processor.*
3. *The PEG ports do not support bifurcation.*
4. *Variants with P-series or U-series processors support either a PCIe x4 Gen 4 port for COM Express PEG port or a PCIe x4 Gen 4 port for optional on-module SSD storage (BOM option)*

5.3 Display Interfaces

The conga-TC675r offers the display combinations and resolutions listed in the table below:

Table 11 Display Combination and Resolution

Display 1 (DDI1) [1]		Display 2 (DDI2) [1]		Display 3 (DDI3)		Display 4 [3]		Display 5	
Interface	Max. Resolution	Interface	Max. Resolution	Interface	Max. Resolution	Interface	Max. Resolution	Interface	Max. Resolution
DP++	up to HBR3 (8.1 Gbps) [2]	DP++	up to HBR3 (8.1 Gbps) [2]	DP++	up to HBR3 (8.1 Gbps) [2]	LVDS or eDP	up to 1920x1200 @ 60 Hz, 18/24 bit (dual LVDS bus mode) up to HBR3 (8.1 Gbps) [2]	VGA (BOM Option) [4]	up to 1920x1200 @ 60 Hz or 2048x1152 @ 60 Hz with reduced blanking

Note

1. *DDI1 is shared with USB4 port 1 and DDI2 is shared with USB4 port 2. For USB4 support, a customized BIOS is required.*
2. *HBR3 supports a max. resolution of 4096x2304 @ 60 Hz, 36 bpp / 5120x3200 @ 60 Hz, 24 bpp* ***without DSC*** *and 5120x3200 @ 120 Hz, 30 bpp / 7680x4320 @ 60 Hz, 30 bpp* ***with DSC*** *(may consume two display pipes).*
3. *The LVDS/eDP interface does not support both LVDS and eDP signals at the same time.*
4. *For VGA support, you need a customized conga-TC675r variant. Additionally, the VGA option must be enabled in BIOS setup to function.*

5.3.1 DP++

The conga-TC675r offers up to three independent DP++ interfaces by default, supporting:

- up to HBR3 (8.1 Gbps)
- VESA DisplayPort Standard 1.4 over native DP connector
- various audio formats

Note

1. *DDI1 is shared with USB4 port 1 and DDI2 is shared with USB4 port 2. For USB4 support, a customized BIOS is required.*
2. *For supported resolutions, see Table 11 "Display Combination and Resolution" above.*

5.3.2 LVDS/eDP

The conga-TC675r offers an LVDS/eDP interface. This interface is configured in the BIOS to support LVDS by default. For eDP support, go to Advanced -> Graphics -> Active LFP Configuration in the BIOS setup menu and select “eDP”.

The LVDS interface supports:

- single or dual channel LVDS (color depths of 18 bpp or 24 bpp)
- integrated flat panel interface with clock frequency up to 112 MHz
- VESA and JEIDA LVDS color mappings
- automatic panel detection via Embedded Panel Interface based on VESA EDID™ 1.3

The eDP interface supports:

- up to HBR3 (8.1 Gbps)
- eDP 1.4b specification
- Spread-Spectrum Clocking

Note

1. *The LVDS/eDP interface does not support both LVDS and eDP signals at the same time.*
2. *For supported resolutions, see Table 11 “Display Combination and Resolution” above.*

5.3.3 Optional VGA

Optionally, the conga-TC675r can support VGA (BOM option), supporting:

- analog RGB output for VGA with Triple 9-bit DAC up to 200MHz pixel rate, separated/composite sync signals

Note

For VGA support, you need a customized conga-TC675r variant. Additionally, the VGA option must be enabled in BIOS setup to function.

5.4 SATA

The conga-TC675r offers two SATA interfaces (SATA 0-1) on the A–B connector. The interfaces support:

- SATA specification revision 3.2
- Independent DMA operation
- data transfer rates up to 6.0 Gb/s
- AHCI mode using memory space and RAID mode
- Intel Rapid Storage Technology
- Hot-plug capable

Note

1. *SATA0 is multiplexed with PCIe7 while SATA1 is multiplexed with PCIe6.*
2. *To ensure reliable SATA operation, disconnect any unused PCIe devices from the multiplexed interface while the SATA device is in use.*
3. *Multiplexing is software controlled in BIOS menu. SATA is enabled by default.*
4. *The interface does not support legacy mode using I/O space.*

5.5 USB 2.0

The conga-TC675r offers signals for up to **eight USB 2.0 ports**.

Note

1. *Each USB 2.0 port is backward compatible with lower link rates (Full-Speed, Low-Speed).*
2. *Each USB 3.2 and USB4 port consumes the signal pair of one USB 2.0 port, thereby reducing the number of available USB 2.0 ports.*

5.6 USB 3.2

The conga-TC675r offers SuperSpeed signals for **up to four USB 3.2 ports**, each supporting up to **USB 3.2 Gen 2x1 (10 Gbps)**.

Note

1. *Each USB 3.2 port is backward compatible with lower link rates, including USB 3.2 Gen 1x1 (5 Gbps), USB 2.0, and USB 1.1.*
2. *Each USB 3.2 port consumes the data pair of one USB 2.0 port, thereby reducing the number of available USB 2.0 ports.*

5.7 Optional USB4

Optionally, the conga-TC675r offers SuperSpeed signals for **up to two USB4 Gen 3x2 ports** (**requires a customized BIOS**) instead of two DDI. Each USB4 port supports a **two-lane configuration** (Data Pairs 0 and 1) and operates in multiple modes, as shown in the table below:

Table 12 Supported Configurations per USB4 Port

Lane 1 (Data Pair 0)	Lane 2 (Data Pair 1)	Description
USB4	USB4	Up to **USB4 Gen 3x2 (40 Gbps)**, including support for non-rounded link rates (10.3125 Gbps / 20.625 Gbps)
USB 3.2	USB 3.2	Up to **USB 3.2 Gen 2x2 (20 Gbps)**
USB 3.2	N.C.	Up to **USB 3.2 Gen 2x1 (10 Gbps)** using a single lane
N.C.	USB 3.2	
USB 3.2	DPx2	Up to **USB 3.2 Gen 2x1 (10 Gbps)** + **Two-lane DisplayPort** over USB-C (DPoC), supporting HBR1, HBR2, HBR3, and RBR
DPx2	USB 3.2	
DPx4		**Four-lane DisplayPort** over USB-C (DPoC)

Not supported: *Two DisplayPorts on the same USB4 port.*

Note

1. *Each USB4 port is backward compatible with lower link rates (e.g., USB4 Gen 3x2 is backward compatible with Gen 2x2 and Gen 2x1).*
2. *DDI1 is shared with USB4 port 1 and DDI2 is shared with USB4 port 2. For USB4 support, a customized BIOS is required.*
3. *Each USB4 port consumes the data pair of one USB 2.0 port, thereby reducing the number of available USB 2.0 ports. For USB4 port 1, use the data pairs of USB 2.0 port 4. For USB4 port 2, use the data pairs of USB 2.0 port 5.*
4. *To enable USB4 functionality, the carrier board must include a Power Delivery (PD) controller and a USB4 retimer, each configured with specific SMLink addresses. For implementation details, contact congatec technical support.*

USB PD controllers and retimers implemented on the carrier board must use the SMLink addresses listed in the table below:

Table 13 USB PD Controller and Retimer Addresses

USB4 Port	1	2
USB PD Controller:		
- SML1 Address (7-bit)	0x21	0x25
- USB_PD_I2C Address(7-bit)	0x22	0x26
Thunderbolt Retimer:		
- SML0 Address (7-bit)	0x54	0x55

5.8 NBASE-T Ethernet

The conga-TC675r offers a 2.5 Gigabit Ethernet interface via an onboard Intel® i226-IT controller [1]. The interface supports:

- full-duplex operation at 10/100/1000/2500 Mbps [2,3]
- half-duplex operation at 10/100 Mbps [2,3]
- Time Sensitive Networking [4]

The table below describes the LED signals of NBASE-T Ethernet interface.

Table 14 NBASE-T Ethernet LED Description

Signals	Description
GBE0_ACT#	Ethernet controller activity indicator
GBE0_LINK# [2,3]	Ethernet controller link indicator
GBE0_LINK_MID#	Ethernet controller link indicator for 1000 Mbps (lower link speed)
GBE0_LINK_MAX#	Ethernet controller link indicator for 2500 Mbps (maximum link speed)

Note

1. *The MAC address of the Intel i226 Ethernet controller is preprogrammed by default. The MAC address cannot be reprogrammed. If you require custom MAC address, contact your local sales representative.*
2. *The GBE0_LINK# output is not active during a 10 Mb and 100 Mb connection. It is only active during a 1 Gb or 2.5 Gb connection. This is a limitation of Ethernet controller since it has only three LED outputs.*
3. *The GBE0_LINK# signal is a logic AND of the GBE0_LINK_MID# and GBE0_LINK_MAX# signals on the conga-TC675r module.*
4. *Not supported in Windows Operating Systems.*

5.9 High Definition Audio

The conga-TC675r provides an HD audio interface on the A–B connector. Alternatively, the conga-TC675r can provide Soundwire interface via an assembly option.

Note

1. *The HDA_SDIN2 signal is not supported.*

5.10 General Purpose SPI

The conga-TC675r offers a general purpose SPI interface via the congatec Board Controller. The interface offers one chip select pin.

5.11 SPI

The conga-TC675r offers the SPI bus through the integrated PCH. The bus supports SPI-compatible flash devices. You can boot the conga-TC675r from the carrier board if you integrate an off-module flash device (BIOS) on the carrier board. This implementation is especially useful when evaluating a customized BIOS.

The conga-TC675r discrete SPI TPM (Infineon SLB9672 FW15) and the congatec BIOS flash are connected to the SPI interface.

Note

This SPI bus is for external BIOS flash only.

5.11.1 BIOS Flash Selection

The boot select pins BIOS_DIS0# and BIOS_DIS1# are configured to load the firmware BIOS from the conga-TC675r by default. Optionally, you can configure these pins to load the boot firmware from the carrier board flash as described in the table below.

Table 15 BIOS Select Options

BIOS_DIS1#	BIOS_DIS0#	Boot Option
0	0	Boot from module SPI flash (default)
0	1	Boot from carrier board SPI flash

5.12 UART

The conga-TC675r offers two standard UART interfaces (UART0 and UART1) via the cBC by default. These interfaces comply with UART 16550 protocol and they support up to 115200 bps.

The UART1 pins can optionally be rerouted to support CAN bus (assembly option).

Note

The UART interfaces do not support hardware handshake and flow control.

5.13 Optional CAN Bus

The conga-TC675r offers an optional CAN bus via a MCP2518FD from the Board Controller (assembly option). The CAN bus supports:

- ISO 11898-1:2015
- data bit rate up to 8 Mbps
- CAN FD, mixed CAN 2.0B and CAN 2.0B modes

Note

1. *CAN bus is available only via a customized conga-TC675r.*
2. *UART1 is not supported if CAN bus is implemented.*
3. *Use a congatec CAN bus driver. For more information, contact congatec technical support.*
4. *This optional CAN bus is not supported in Microsoft® Windows®*

5.14 I²C Bus

The I²C bus is implemented through the congatec board controller and accessed using the congatec CGOS driver and API. The cBC provides a fast-mode, multi-master I²C bus with maximum I²C bandwidth.

Table 16 Reserved I2C Addresses

8-bit Device Address	7-bit Device Address	Device	Description
0xAE	0x57	Carrier board EEPROM	Reserved for COM Express® carrier board EEPROM
0x14	0x0A	congatec Board Controller	Reserved for battery management
0x16	0x0B	congatec Board Controller	Reserved for battery management

Note

1. *Use the congatec CGOS driver and API to access the I²C bus.*
2. *Onboard resources are not connected to the I²C bus.*

5.15 LPC Bus

The conga-TC675r offers the LPC bus through an eSPI to LPC bridge. For information about the decoded LPC addresses, see section 9 “System Resources”.

Note

The LPC bus runs at 24 MHz.

5.16 GPIOs

The conga-TC675r offers eight General Purpose Input/Output signals on the A–B connector via the congatec Board Controller.

5.17 SMBus

The conga-TC675r offers the System Management Bus (SMBus) via the congatec Board Controller by default. Optionally, you can route the SMBus signals from the SoC instead (via an isolation switch) by configuring the routing in the BIOS setup menu.

Table 17 Reserved SMBus Addresses

8-bit Device Address	7-bit Device Address	Device	Comment
0x6C 0x6E 0xA0 0xA2 0xA4	0x36 0x37 0x50 0x51 0x52	Memory SPD EEPROM	
0x30 0x32 0x34	0x18 0x19 0x1A	Memory temperature sensor	
0xC0	0x60	eDP to LVDS bridge	If SMBus Isolation switch in BIOS is set to "Never"
0x14 0x16	0x0A 0x0B	congatec Board Controller	Reserved for battery management

Note

1. *Do not use the SMBus for off-board non-system management devices. For more information, contact congatec technical support.*
2. *Make sure the address space of the carrier board SMBus devices does not overlap the address space of the module devices. For more information, refer to the COM Express® Module Base Specification and Carrier Design Guide.*

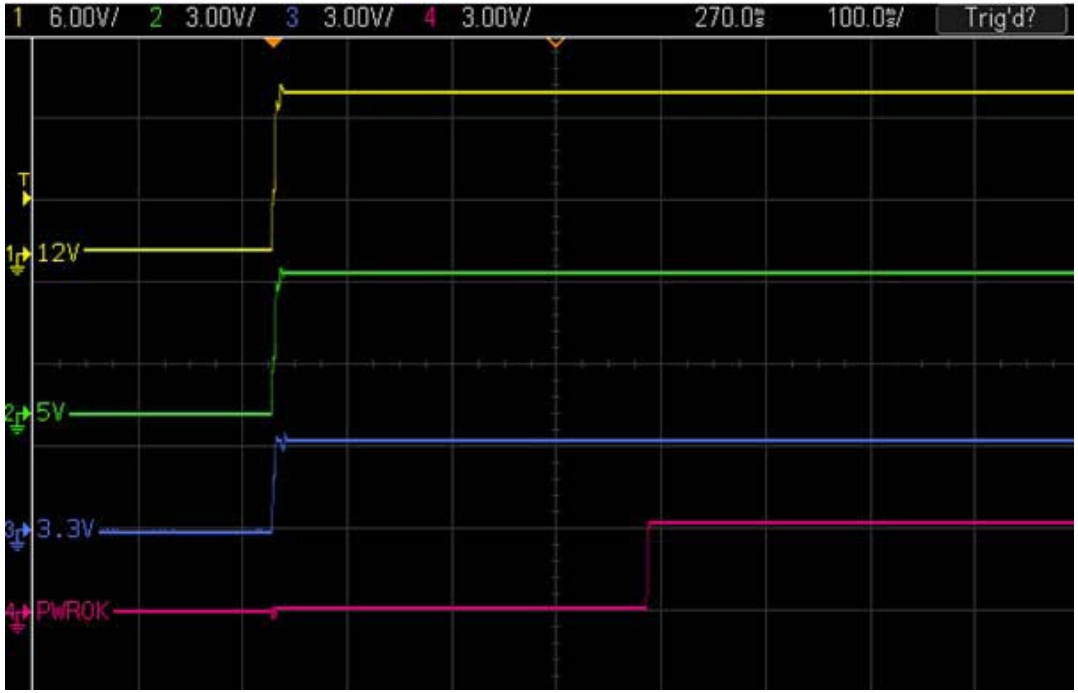
5.18 Power Control

PWR_OK

Power OK from main power supply or carrier board voltage regulator circuitry. A high value indicates that the power is good and the module can start its onboard power sequencing.

Carrier board hardware must drive this signal low until all power rails and clocks are stable. Releasing PWR_OK too early or not driving it low at all can cause numerous boot up problems. It is a good design practice to delay the PWR_OK signal a little (typically 100ms) after all carrier board power rails are up, to ensure a stable system.

A sample screenshot is shown below:



The module will remain in power-off state as long as the PWR_OK is driven by carrier board hardware.The conga-TC675r supports the controlling of ATX-style power supplies. If you do not use an ATX power supply, do not connect the conga-TC675r pins SUS_S3, 5V_SB, and PWRBTN#.

SUS_S3#

The SUS_S3# (pin A15 on the A–B connector) signal is an active-low output that can be used to turn on the main outputs of an ATX-style power supply. To accomplish this the signal must be inverted with an inverter/transistor that is supplied by standby voltage and is located on the carrier board.

PWRBTN#

When using ATX-style power supplies, PWRBTN# (pin B12 on the A–B connector) is used to connect to a momentary-contact, active-low debounced push-button input while the other terminal on the push-button must be connected to ground. This signal is internally pulled up to 3V_VSB using a 20 kΩ resistor. When PWRBTN# is asserted it indicates that an operator wants to turn the power on or off. The response to this signal from the system may vary as a result of modifications made in BIOS settings or by system software.

Power Supply Implementation Guidelines

The 12 V input power is the sole operational power source for the conga-TC675r. The other voltages required are generated internally on the module using onboard voltage regulators.

Note

When designing a power supply for a conga-TC675r application, be aware that the system may malfunction when a 12 V power supply that produces non-monotonic voltage is used to power the system up. Though this problem is rare, it has been observed in some mobile power supply applications.

This problem occurs because some internal circuits on the module (e.g. clock-generator chips) generate their own reset signals when the supply voltage exceeds a certain voltage threshold. A voltage dip after passing this threshold may lead to these circuits becoming confused, thereby resulting in a malfunction.

To ensure this problem does not occur, observe the power supply rise waveform through an oscilloscope, during the power supply qualification phase. This will help to determine if the rise is indeed monotonic and does not have any dips. For more information, see the "Power Supply Design Guide for Desktop Platform Form Factors" document at www.intel.com.

5.18.1 Power Management

ACPI

The conga-TC675r supports Advanced Configuration and Power Interface (ACPI) specification, revision 6.0. It also supports Suspend to RAM (S3). For more information, see section 7.5 “ACPI Suspend Modes and Resume Events”.

S5e Power State

The conga-TC675r features a congatec proprietary Enhanced Soft-Off power state. See section 6.1.5 “Enhanced Soft-Off State” for more information.

5.18.2 Inrush Current

The inrush current of the conga-TC675r is listed below.

Table 18 Inrush Current

Power Rail	Current [A]	Slew Rate [kV/s]	Voltage Ramp [ms]	Comment
VCC_12V	32.00	20.168	0.476	Typical scenario
VCC_5V_SBY	10.00	9.746	0.985	
VCC_12V	11.88	31.008	0.129	Worst-case scenario
VCC_5V_SBY	1.28	3.922	1.020	

Note

Ensure the power supply and decoupling capacitors on the carrier board are adequate for proper power sequencing.

6 Additional Features

The following additional features are available on the conga-TC675r.

6.1 congatec Board Controller (cBC)

The conga-TC675r is equipped with Microchip MEC1706 microcontroller. This onboard microcontroller plays an important role for most of the congatec embedded/industrial PC features. It fully isolates some of the embedded features such as system monitoring or I²C bus from the x86 core architecture, resulting in higher performance and reliability, even when the x86 processor is in a low power mode. It also ensures that the congatec embedded feature set is fully compatible amongst all congatec modules.

The board controller supports the following features:

- Board information
- General Purpose Input/Output (see the section 5.16 “GPIOs”)
- Watchdog
- I²C bus (see the section 5.14 “I²C Bus”)
- SMBus (see the section 5.17 “SMBus”)
- UART (see the section section 5.12 “UART”)
- Power loss control
- Fan control
- Enhanced soft-off state (S5e)
- General Purpose SPI (see the section 1 “The HDA_SDIN2 signal is not supported.”)
- User EEPROM space

6.1.1 Board Information

The cBC provides a rich data-set of manufacturing and board information such as serial number, EAN number, hardware and firmware revisions, and so on. It also keeps track of dynamically changing data like runtime meter and boot counter.

6.1.2 Watchdog

The conga-TC675r is equipped with a multi stage watchdog solution that is triggered by software. For more information about the Watchdog feature, see the application note AN3_Watchdog.pdf on the congatec GmbH website at www.congatec.com

Note

The conga-TC675r module does not support the watchdog NMI mode.

6.1.3 Power Loss Control

The cBC provides the power loss control feature. The power loss control feature determines the behaviour of the system after an AC power loss occurs. This feature applies to systems with ATX-style power supplies which support standby power rail.

The term "power loss" implies that all power sources, including the standby power are lost (G3 state). Once power loss (transition to G3) or shutdown (transition to S5) occurs, the board controller continuously monitors the standby power rail. If the standby voltage remains stable for 30 seconds, the cBC assumes the system was switched off properly. If the standby voltage is no longer detected within 30 seconds, the module considers this an AC power loss condition.

The power loss control feature has three different modes that define how the system responds when standby power is restored after a power loss occurs. The modes are:

- Turn On: The system is turned on after a power loss condition
- Remain Off: The system is kept off after a power loss condition
- Last State: The board controller restores the last state of the system before the power loss condition

Note

1. *If a power loss condition occurs within 30 seconds after a regular shutdown, the cBC may incorrectly set the last state to "ON".*
2. *The settings for power loss control have no effect on systems with AT-style power supplies which do not support standby power rail.*
3. *The 30 seconds monitoring cycle applies only to the "Last State" power loss control mode.*

6.1.4 Fan Control

The conga-TC675r offers FAN_PWMOUT output signal and FAN_TACHOIN input signal for fan control, thereby improving system management. The FAN_PWMOUT signal controls the system fan with PWM (Pulse Width Modulation) while the FAN_TACHOIN signal provides the ability to monitor the system's fan RPMs (revolutions per minute).

The FAN_TACHOIN signal must receive two pulses per revolution in order to produce an accurate reading. For this reason, a two-pulse per revolution fan or similar hardware solution is recommended.

Note

1. *A four wire fan must be used to generate the correct speed readout.*

2. *For the correct fan control (FAN_PWMOUT, FAN_TACHIN) implementation, see the COM Express® Design Guide.*

6.1.5 Enhanced Soft-Off State

The conga-TC675r supports an enhanced Soft-Off state (S5e)—a congatec proprietary low-power Soft-Off state. In this state, the CPU module switches off almost all the onboard logic in order to reduce the power consumption to absolute minimum (between 0.05 mA and 0.09 mA).

Refer to congatec application note AN36_S5e_Implementation.pdf for detailed description of the S5e state.

6.2 OEM BIOS Customization

The conga-TC675r is equipped with congatec Embedded BIOS, which is based on American Megatrends Inc. Aptio UEFI firmware. The congatec Embedded BIOS allows system designers to modify the BIOS. For more information about customizing the congatec Embedded BIOS, refer to the congatec System Utility user's guide CGUTLm1x.pdf on the congatec website at www.congatec.com or contact technical support.

The customization features supported are described below:

6.2.1 OEM Default Settings

This feature allows system designers to create and store their own BIOS default configuration. Customized BIOS development by congatec for OEM default settings is no longer necessary because customers can easily perform this configuration by themselves using the congatec system utility CGUTIL. See congatec application note AN8_Create_OEM_Default_Map.pdf on the congatec website for details on how to add OEM default settings to the congatec Embedded BIOS.

6.2.2 OEM Boot Logo

This feature allows system designers to replace the standard text output displayed during POST with their own BIOS boot logo. Customized BIOS development by congatec for OEM Boot Logo is no longer necessary because customers can easily perform this configuration by themselves using the congatec system utility CGUTIL. See congatec application note AN8_Create_And_Add_Bootlogo.pdf on the congatec website for details on how to add OEM boot logo to the congatec Embedded BIOS.

6.2.3 OEM POST Logo

This feature allows system designers to replace the congatec POST logo displayed in the upper left corner of the screen during BIOS POST with their own BIOS POST logo. Use the congatec system utility CGUTIL 1.5.4 or later to replace/add the OEM POST logo.

6.2.4 OEM DXE Driver

This feature allows designers to add their own UEFI DXE driver to the congatec embedded BIOS. Contact congatec technical support for more information on how to add an OEM DXE driver.

6.3 congatec Battery Management Interface

To facilitate the development of battery powered mobile systems based on embedded modules, congatec GmbH defined an interface for the exchange of data between a CPU module (using an ACPI operating system) and a Smart Battery system. A system developed according to the congatec Battery Management Interface Specification can provide the battery management functions supported by an ACPI capable operating system (for example, charge state of the battery, information about the battery, alarms/events for certain battery states and so on) without the need for additional modifications to the system BIOS.

In addtion to the ACPI-Compliant Control Method Battery mentioned above, the latest versions of the conga-TC675r BIOS and board controller firmware also support LTC1760 battery manager from Linear Technology and a battery only solution (no smart battery system manager). All three battery solutions are supported on the I2C bus and the SMBus. This gives the system designer more flexibility when choosing the appropriate battery sub-system. For more information about the supported Battery Management Interface, contact your local sales representative.

6.4 API Support (CGOS)

In order to benefit from the above mentioned non-industry standard feature set, congatec provides an API that allows application software developers to easily integrate all these features into their code. The CGOS API (congatec Operating System Application Programming Interface) is the congatec proprietary API that is available for all commonly used Operating Systems such as Win32, Win64, Win CE, Linux. The architecture of the CGOS API driver provides the ability to write application software that runs unmodified on all congatec CPU modules. All the hardware related code is contained within the congatec embedded BIOS on the module. See section 1.1 of the CGOS API software developers guide, available on the congatec website.

6.5 Security Features

The conga-TC675r offers a discrete SPI TPM 2.0 (Infineon SLB9672 FW15) by default.

6.6 Suspend to RAM/Disk

The Suspend to RAM and Suspend to Disk features are supported on the conga-TC675r.

7 conga Tech Notes

The conga-TC675r has some technological features that require additional explanation. The following section will give the reader a better understanding of some of these features.

7.1 Adaptive Thermal Monitor and Catastrophic Thermal Protection

Intel® Xeon, Core™ i7/i5/i3 and Celeron® and Pentium® processors have a thermal monitor feature that helps to control the processor temperature. The integrated TCC (Thermal Control Circuit) activates if the processor silicon reaches its maximum operating temperature. The activation temperature that the Intel® Thermal Monitor uses to activate the TCC can be slightly modified via TCC Activation Offset in BIOS setup submenu "CPU submenu".

The Adaptive Thermal Monitor controls the processor temperature using two methods:

- Adjusting the processor's operating frequency and core voltage (EIST transitions)
- Modulating (start/stop) the processor's internal clocks at a duty cycle of 25% on and 75% off

When activated, the TCC causes both processor core and graphics core to reduce frequency and voltage adaptively. The Adaptive Thermal Monitor will remain active as long as the package temperature remains at its specified limit. Therefore, the Adaptive Thermal Monitor will continue to reduce the package frequency and voltage until the TCC is de-activated. Clock modulation is activated if frequency and voltage adjustments are insufficient. Additional hardware, software driver, or operating system support is not required.

Intel®'s Core™ i7/i5/i3, Celeron® and Pentium® processors use the THERMTRIP# signal to shut down the system if the processor's silicon reaches a temperature of approximately 125°C. The THERMTRIP# signal activation is completely independent from processor activity and therefore does not produce any bus cycles.

Note

1. *The maximum operating temperature for Intel® Core™ i7/i5/i3, Celeron® and Pentium® processors is 100°C*

2. *To ensure that the TCC is active for only short periods of time, thus reducing the impact on processor performance to a minimum, it is necessary to have a properly designed thermal solution. The Intel® Core™ i7/i5/i3, Celeron® and Pentium® processor's respective datasheet can provide you with more information about this subject.*

7.2 Processor Performance Control

7.2.1 Intel® SpeedStep® Technology (EIST)

Intel® processors found on the conga-TC675r run at different voltage/frequency states (performance states), which is referred to as Enhanced Intel® SpeedStep® Technology (EIST). Operating systems that support performance control take advantage of microprocessors that use several different performance states to efficiently operate the processor when it is not being fully used. The operating system will determine the necessary performance state that the processor should run at so that the optimal balance between performance and power consumption can be achieved during runtime.

The Windows family of operating systems links its processor performance control policy to the power scheme setting. You must ensure that the power scheme setting you choose has the ability to support Enhanced Intel® SpeedStep® technology.

The 13th Generation Intel® Core™ processor family supports Intel Speed Shift, a new and energy efficient method for frequency control. This feature is also referred to as Hardware-controlled Performance States (HWP). The feature is a hardware implementation of the ACPI defined Collaborative Processor Performance Control (CPPC2) and is supported by newer operating systems (Win 8.1 or newer).

With this feature enabled, the processor autonomously selects performance states based on workload demand and thermal limits while also considering information provided by the OS e.g., the performance limits and workload history.

7.2.2 Intel® Turbo Boost Technology

Intel® Turbo Boost Technology allows processor cores to run faster than the base operating frequency if it is operating below power, current, and temperature specification limits. Intel® Turbo Boost Technology is activated when the Operating System (OS) requests the highest processor performance state. The maximum frequency of Intel® Turbo Boost Technology depends on the number of active cores. The amount of time the processor spends in the Intel Turbo Boost Technology state depends on the workload and operating environment.

Any of the following can set the upper limit of Intel® Turbo Boost Technology on a given workload:

- Number of active cores
- Estimated current consumption
- Estimated power consumption
- Processor temperature

When the processor is operating below these limits and the user's workload demands additional performance, the processor frequency dynamically increases by 100 MHz on short and regular intervals until the upper limit is met or the maximum possible upside for the number of active cores is reached.

For more information about Intel® Turbo Boost Technology, visit the Intel® website.

Note

1. *For real-time sensitive applications, disable EIST and Turbo Mode in the BIOS setup to ensure a more deterministic performance.*

2. *Disable Turbo mode for industrial use condition.*

7.3 Intel® Virtualization Technology

Intel® Virtualization Technology (Intel® VT) makes a single system appear as multiple independent systems to software. With this technology, multiple, independent operating systems can run simultaneously on a single system. The technology components support virtualization of platforms based on Intel architecture microprocessors and chipsets.

Intel® Virtualization Technology for IA-32, Intel® 64 and Intel® Architecture (Intel® VT-x) have hardware support in the processor to improve the virtualization performance and robustness.

RTS Real-Time Hypervisor supports Intel VT and is verified on all current congatec x86 hardware.

Note

congatec supports RTS Hypervisor.

7.4 Thermal Management

ACPI is responsible for allowing the operating system to play an important part in the system's thermal management. This results in the operating system having the ability to implement cooling decisions according to the demands of the application.

The conga-TC675r offers hardware-based support for passive and active cooling. Passive cooling is implemented in the Intel CPU via the Thermal Control Circuit (TCC) Activation Offset setting in the CPU configuration setup sub-menu. The TCC in the processor is activated at 100°C by default but can be lowered by the Activation Offset—for example, an activation offset of "10" will activate TCC at 90°C. ACPI OS support is not required. See section 7.1 "Adaptive Thermal Monitor and Catastrophic Thermal Protection" for more information.

The congatec board controller supports active cooling solution. The board controller controls the fan's speed based on the temperature readings of the CPU. This feature does not require ACPI OS support. The only software-controlled thermal trip point on conga-TC675r is the Critical Trip Point.

The active or passive cooling policy should ensure that the CPU temperature does not reach this trip point. However, if the critical trip point is reached, the OS will shut down properly in order to prevent damage to the system.

Use the "critical trip point" setup node in the BIOS setup menu to determine the temperature threshold at which the system shuts down.

Note

The Automatic Critical Trip Point BIOS setting shuts down the system at 5°C above the maximum specified temperature of the processor

7.5 ACPI Suspend Modes and Resume Events

The conga-TC675r BIOS supports S3 (Suspend to RAM), S4 (Suspend to Disk), S5 (Soft-Off) and S5e (enhanced Soft-Off).

Table 19 Wake Events

The table below lists the events that wake the system from S3-S5 and S5e.

Wake Event	Conditions/Remarks
Power Button	Wakes unconditionally from S3-S5, S5e.
Onboard LAN Event	Device driver must be configured for Wake On LAN support.
SMBALERT#	Wakes unconditionally from S3-S5, S5e.
PCI Express WAKE#	Wakes unconditionally from S3-S5.
WAKE#	Wakes unconditionally from S3, S4.
PME#	Activate the wake up capabilities of a PCI device using Windows Device Manager configuration options for this device OR set Resume On PME# to Enabled in the Power setup menu.
USB Mouse/Keyboard Event	When Standby mode is set to S3 or S4, USB hardware must be powered by standby power source. Set USB Device Wakeup from S3/S4 to "Enabled" in the ACPI setup menu (if this BIOS option is available). In Device Manager look for the keyboard/mouse devices. Go to the Power Management tab and check 'Allow this device to bring the computer out of standby'.
RTC Alarm	Activate and configure Resume On RTC Alarm in the Power setup menu. Only available in S5.
Watchdog Power Button Event	Wakes unconditionally from S3-S5.

8 Signal Descriptions and Pinout Tables

The following section describes the signals found on COM Express® Type 6 connectors used for congatec GmbH modules. The pinout of the modules complies with COM Express® Type 6, rev. 3.1.

The table below describes the terminology used in this section. The PU/PD column indicates if a pull-up or pull-down resistor has been used. If the field entry area in this column for the signal is empty, then no pull-up or pull-down resistor has been implemented by congatec.

The "#" symbol at the end of the signal name indicates that the active or asserted state occurs when the signal is at a low voltage level. When "#" is not present, the signal is asserted when at a high voltage level.

Table 20 Signal Tables Terminology Descriptions

Term	Description
DDC	Display Data Channel
I/O 3.3V	Bi-directional signal 3.3 V tolerant
I/O 5V	Bi-directional signal 5 V tolerant
I 3.3V	Input 3.3 V tolerant
I 5V	Input 5 V tolerant
I/O 3.3VSB	Input or output 3.3 V tolerant active in standby state
LVDS	Low Voltage Differential Signal - 330 mV nominal; 450 mV maximum differential signal
O 3.3V	Output 3.3 V signal level
O 5V	Output 5 V signal level
OD	Open drain output
P	Power Input/Output
PCIE	PCI Express compatible differential signal. In compliance with PCI Express Specification.
PD	Implemented pull-down resistor
PDS	Pull-down strap. A module output pin that is either tied to GND or is not connected. Used to signal module capabilities (pinout type) to the carrier board.
PEG	PCI Express Graphics
PU	Implemented pull-up resistor
REF	Reference voltage output. May be sourced from a module power plane.
SATA	In compliance with Serial ATA specification revision 2.6 and 3.0.
USB_SS	USB Super Speed compliant signals. This includes USB 3.0, USB 3.1, USB 3.2 and USB4.

8.1 Connector Signal Descriptions

Table 21 Connector A–B Pinout

Pin	Row A	Pin	Row B	Pin	Row A	Pin	Row B
A1	GND (FIXED)	B1	GND (FIXED)	A56	PCIE_TX4-	B56	PCIE_RX4-
A2	GBE0_MDI3-	B2	GBE0_ACT#	A57	GND	B57	GPO2
A3	GBE0_MDI3+	B3	LPC_FRAME#	A58	PCIE_TX3+	B58	PCIE_RX3+
A4	GBE0_LINK_MID#	B4	LPC_AD0	A59	PCIE_TX3-	B59	PCIE_RX3-
A5	GBE0_LINK_MAX#	B5	LPC_AD1	A60	GND (FIXED)	B60	GND (FIXED)
A6	GBE0_MDI2-	B6	LPC_AD2	A61	PCIE_TX2+	B61	PCIE_RX2+
A7	GBE0_MDI2+	B7	LPC_AD3	A62	PCIE_TX2-	B62	PCIE_RX2-
A8	GBE0_LINK#	B8	LPC_DRQ0# [1]	A63	GPI1	B63	GPO3
A9	GBE0_MDI1-	B9	LPC_DRQ1# [1]	A64	PCIE_TX1+	B64	PCIE_RX1+
A10	GBE0_MDI1+	B10	LPC_CLK/ESPI_CK	A65	PCIE_TX1-	B65	PCIE_RX1-
A11	GND (FIXED)	B11	GND (FIXED)	A66	GND	B66	WAKE0#
A12	GBE0_MDI0-	B12	PWRBTN#	A67	GPI2	B67	WAKE1#
A13	GBE0_MDI0+	B13	SMB_CK	A68	PCIE_TX0+	B68	PCIE_RX0+
A14	GBE0_CTREF [1]	B14	SMB_DAT	A69	PCIE_TX0-	B69	PCIE_RX0-
A15	SUS_S3#	B15	SMB_ALERT#	A70	GND (FIXED)	B70	GND (FIXED)
A16	SATA0_TX+	B16	SATA1_TX+	A71	eDP_TX2+/LVDS_A0+	B71	LVDS_B0+
A17	SATA0_TX-	B17	SATA1_TX-	A72	eDP_TX2-/LVDS_A0-	B72	LVDS_B0-
A18	SUS_S4#	B18	SUS_STAT#	A73	eDP_TX1+/LVDS_A1+	B73	LVDS_B1+
A19	SATA0_RX+	B19	SATA1_RX+	A74	eDP_TX1-/LVDS_A1-	B74	LVDS_B1-
A20	SATA0_RX-	B20	SATA1_RX-	A75	eDP_TX0+/LVDS_A2+	B75	LVDS_B2+
A21	GND (FIXED)	B21	GND (FIXED)	A76	eDP_TX0-/LVDS_A2-	B76	LVDS_B2-
A22	SATA2_TX+ [1]	B22	SATA3_TX+ [1]	A77	eDP_VDD_EN/LVDS_VDD_EN	B77	LVDS_B3+
A23	SATA2_TX- [1]	B23	SATA3_TX- [1]	A78	LVDS_A3+	B78	LVDS_B3-
A24	SUS_S5#	B24	PWR_OK	A79	LVDS_A3-	B79	eDP_BKLT_EN/LVDS_BKLT_EN
A25	SATA2_RX+ [1]	B25	SATA3_RX+ [1]	A80	GND (FIXED)	B80	GND (FIXED)
A26	SATA2_RX- [1]	B26	SATA3_RX- [1]	A81	eDP_TX3+/LVDS_A_CK+	B81	LVDS_B_CK+
A27	BATLOW#	B27	WDT	A82	eDP_TX3-/LVDS_A_CK-	B82	LVDS_B_CK-
A28	(S)_ATA_ACT#	B28	HDA_SDIN2 [2] / SNDW0_CLK [3]	A83	eDP_AUX+/LVDS_I2C_CK	B83	eDP/LVDS_BKLT_CTRL
A29	HDA_SYNC	B29	HDA_SDIN1 / SNDW0_DAT [3]	A84	eDP_AUX-/LVDS_I2C_DAT	B84	VCC_5V_SBY
A30	HDA_RST#	B30	HDA_SDIN0	A85	GPI3	B85	VCC_5V_SBY

Pin	Row A	Pin	Row B	Pin	Row A	Pin	Row B
A31	GND (FIXED)	B31	GND (FIXED)	A86	GP_SPI_MOSI	B86	VCC_5V_SBY
A32	HDA_BITCLK	B32	SPKR	A87	eDP_HPD	B87	VCC_5V_SBY
A33	HDA_SDOUT	B33	I2C_CK	A88	PCIE_CLK_REF+	B88	BIOS_DIS1#
A34	BIOS_DIS0#	B34	I2C_DAT	A89	PCIE_CLK_REF-	B89	VGA_RED [3]
A35	THRMTRIP#	B35	THRM#	A90	GND (FIXED)	B90	GND (FIXED)
A36	USB6-	B36	USB7-	A91	SPI_POWER	B91	VGA_GRN [3]
A37	USB6+	B37	USB7+	A92	SPI_MISO	B92	VGA_BLU [3]
A38	USB_6_7_OC#	B38	USB_4_5_OC#	A93	GPO0	B93	VGA_HSYNC [3]
A39	USB4-	B39	USB5-	A94	SPI_CLK	B94	VGA_VSYNC [3]
A40	USB4+	B40	USB5+	A95	SPI_MOSI	B95	VGA_I2C_CK [3]
A41	GND (FIXED)	B41	GND (FIXED)	A96	TPM_PP [2]	B96	VGA_I2C_DAT [3]
A42	USB2-	B42	USB3-	A97	TYPE10# [1]	B97	SPI_CS#
A43	USB2+	B43	USB3+	A98	SER0_TX	B98	GP_SPI_MISO
A44	USB_2_3_OC#	B44	USB_0_1_OC#	A99	SER0_RX	B99	GP_SPI_CK
A45	USB0-	B45	USB1-	A100	GND (FIXED)	B100	GND (FIXED)
A46	USB0+	B46	USB1+	A101	SER1_TX	B101	FAN_PWMOUT
A47	VCC_RTC	B47	ESPI_EN# [1]	A102	SER1_RX	B102	FAN_TACHIN
A48	RSMRST_OUT#	B48	USB0_HOST_PRSNT	A103	LID#	B103	SLEEP#
A49	GBE0_SDP	B49	SYS_RESET#	A104	VCC_12V	B104	VCC_12V
A50	LPC_SERIRQ	B50	CB_RESET#	A105	VCC_12V	B105	VCC_12V
A51	GND (FIXED)	B51	GND (FIXED)	A106	VCC_12V	B106	VCC_12V
A52	PCIE_TX5+	B52	PCIE_RX5+	A107	VCC_12V	B107	VCC_12V
A53	PCIE_TX5-	B53	PCIE_RX5-	A108	VCC_12V	B108	VCC_12V
A54	GPI0	B54	GPO1	A109	VCC_12V	B109	VCC_12V
A55	PCIE_TX4+	B55	PCIE_RX4+	A110	GND (FIXED)	B110	GND (FIXED)

Note

1. *Not connected*
2. *Not supported*
3. *Assembly option*

Table 22 Connector C–D Pinout

Pin	Row C	Pin	Row D	Pin	Row C	Pin	Row D
C1	GND (FIXED)	D1	GND (FIXED)	C56	PEG_RX1-	D56	PEG_TX1-
C2	GND	D2	GND	C57	TYPE1# [1]	D57	TYPE2#
C3	USB_SSRX0-	D3	USB_SSTX0-	C58	PEG_RX2+	D58	PEG_TX2+
C4	USB_SSRX0+	D4	USB_SSTX0+	C59	PEG_RX2-	D59	PEG_TX2-
C5	GND	D5	GND	C60	GND (FIXED)	D60	GND (FIXED)
C6	USB_SSRX1-	D6	USB_SSTX1-	C61	PEG_RX3+	D61	PEG_TX3+
C7	USB_SSRX1+	D7	USB_SSTX1+	C62	PEG_RX3-	D62	PEG_TX3-
C8	GND	D8	GND	C63	GND	D63	GND
C9	USB_SSRX2-	D9	USB_SSTX2-	C64	GND	D64	GND
C10	USB_SSRX2+	D10	USB_SSTX2+	C65	PEG_RX4+ [3]	D65	PEG_TX4+ [3]
C11	GND (FIXED)	D11	GND (FIXED)	C66	PEG_RX4- [3]	D66	PEG_TX4- [3]
C12	USB_SSRX3-	D12	USB_SSTX3-	C67	RAPID_SHUTDOWN	D67	GND
C13	USB_SSRX3+	D13	USB_SSTX3+	C68	PEG_RX5+ [3]	D68	PEG_TX5+ [3]
C14	GND	D14	GND	C69	PEG_RX5- [3]	D69	PEG_TX5- [3]
C15	USB4_1_LSTX	D15	DDI1_CTRLCLK_AUX+/ USB4_1_AUX+	C70	GND (FIXED)	D70	GND (FIXED)
C16	USB4_1_LSRX	D16	DDI1_CTRLDATA_AUX- / USB4_1_AUX-	C71	PEG_RX6+ [3]	D71	PEG_TX6+ [3]
C17	USB4_RT_ENA	D17	USB4_PD_I2C_ALERT#	C72	PEG_RX6- [3]	D72	PEG_TX6- [3]
C18	GND	D18	PMCALERT# [1]	C73	GND	D73	GND
C19	PCIE_RX6+	D19	PCIE_TX6+	C74	PEG_RX7+ [3]	D74	PEG_TX7+ [3]
C20	PCIE_RX6-	D20	PCIE_TX6-	C75	PEG_RX7- [3]	D75	PEG_TX7- [3]
C21	GND (FIXED)	D21	GND (FIXED)	C76	GND	D76	GND
C22	PCIE_RX7+	D22	PCIE_TX7+	C77	GND	D77	GND
C23	PCIE_RX7-	D23	PCIE_TX7-	C78	PEG_RX8+ [1]	D78	PEG_TX8+ [1]
C24	DDI1_HPD	D24	GND	C79	PEG_RX8- [1]	D79	PEG_TX8- [1]
C25	SML0_CLK	D25	GND	C80	GND (FIXED)	D80	GND (FIXED)
C26	SML0_DAT	D26	DDI1_PAIR0+ / USB4_1_SSTX0+	C81	PEG_RX9+ [1]	D81	PEG_TX9+ [1]
C27	SML1_CLK	D27	DDI1_PAIR0- / USB4_1_SSTX0-	C82	PEG_RX9- [1]	D82	PEG_TX9- [1]
C28	SML1_DAT	D28	GND	C83	GND	D83	GND

Pin	Row C	Pin	Row D	Pin	Row C	Pin	Row D
C29	USB4_PD_I2C_CLK	D29	DDI1_PAIR1+ / USB4_1_SSRX0+	C84	GND	D84	GND
C30	USB4_PD_I2C_DAT	D30	DDI1_PAIR1- / USB4_1_SSRX0-	C85	PEG_RX10+ [1]	D85	PEG_TX10+ [1]
C31	GND (FIXED)	D31	GND (FIXED)	C86	PEG_RX10- [1]	D86	PEG_TX10- [1]
C32	DDI2_CTRLCLK_AUX+ / USB4_2_AUX+	D32	DDI1_PAIR2+ / USB4_1_SSTX1+	C87	GND	D87	GND
C33	DDI2_CTRLDATA_AUX- / USB4_2_AUX-	D33	DDI1_PAIR2- / USB4_1_SSTX1-	C88	PEG_RX11+ [1]	D88	PEG_TX11+ [1]
C34	DDI2_DDC_AUX_SEL	D34	DDI1_DDC_AUX_SEL	C89	PEG_RX11- [1]	D89	PEG_TX11- [1]
C35	USB4_2_LSTX	D35	USB4_2_LSRX	C90	GND (FIXED)	D90	GND (FIXED)
C36	DDI3_CTRLCLK_AUX+	D36	DDI1_PAIR3+ / USB4_1_SSRX1+	C91	PEG_RX12+ [1]	D91	PEG_TX12+ [1]
C37	DDI3_CTRLDATA_AUX-	D37	DDI1_PAIR3- / USB4_1_SSRX1-	C92	PEG_RX12- [1]	D92	PEG_TX12- [1]
C38	DDI3_DDC_AUX_SEL	D38	GND	C93	GND	D93	GND
C39	DDI3_PAIR0+	D39	DDI2_PAIR0+ / USB4_2_SSTX0+	C94	PEG_RX13+ [1]	D94	PEG_TX13+ [1]
C40	DDI3_PAIR0-	D40	DDI2_PAIR0- / USB4_2_SSTX0-	C95	PEG_RX13- [1]	D95	PEG_TX13- [1]
C41	GND (FIXED)	D41	GND (FIXED)	C96	GND	D96	GND
C42	DDI3_PAIR1+	D42	DDI2_PAIR1+ / USB4_2_SSRX0+	C97	GND	D97	GND
C43	DDI3_PAIR1-	D43	DDI2_PAIR1- / USB4_2_SSRX0-	C98	PEG_RX14+ [1]	D98	PEG_TX14+ [1]
C44	DDI3_HPD	D44	DDI2_HPD	C99	PEG_RX14- [1]	D99	PEG_TX14- [1]
C45	GP_SPI_CS#	D45	GND	C100	GND (FIXED)	D100	GND (FIXED)
C46	DDI3_PAIR2+	D46	DDI2_PAIR2+ / USB4_2_SSTX1+	C101	PEG_RX15+ [1]	D101	PEG_TX15+ [1]
C47	DDI3_PAIR2-	D47	DDI2_PAIR2- / USB4_2_SSTX1-	C102	PEG_RX15- [1]	D102	PEG_TX15- [1]
C48	RSVD [1]	D48	GND	C103	GND	D103	GND
C49	DDI3_PAIR3+	D49	DDI2_PAIR3+ / USB4_2_SSRX1+	C104	VCC_12V	D104	VCC_12V
C50	DDI3_PAIR3-	D50	DDI2_PAIR3- / USB4_2_SSRX1-	C105	VCC_12V	D105	VCC_12V
C51	GND (FIXED)	D51	GND (FIXED)	C106	VCC_12V	D106	VCC_12V

Pin	Row C	Pin	Row D	Pin	Row C	Pin	Row D
C52	PEG_RX0+	D52	PEG_TX0+	C107	VCC_12V	D107	VCC_12V
C53	PEG_RX0-	D53	PEG_TX0-	C108	VCC_12V	D108	VCC_12V
C54	TYPE0# [1]	D54	PEG_LANE_RV#	C109	VCC_12V	D109	VCC_12V
C55	PEG_RX1+	D55	PEG_TX1+	C110	GND (FIXED)	D110	GND (FIXED)

Note

1. *Not connected*
2. *Not supported*
3. *PEG 4-7 is not available on variants with P- and U-Series processors.*

Table 23 PCI Express Signal Descriptions (General Purpose)

Signal	Pin #	Description	I/O	PU/PD	Comment
PCIE_RX0+ PCIE_RX0-	B68 B69	PCI Express channel 0, Receive Input differential pair	I PCIE		
PCIE_TX0+ PCIE_TX0-	A68 A69	PCI Express channel 0, Transmit Output differential pair	O PCIE		
PCIE_RX1+ PCIE_RX1-	B64 B65	PCI Express channel 1, Receive Input differential pair	I PCIE		
PCIE_TX1+ PCIE_TX1-	A64 A65	PCI Express channel 1, Transmit Output differential pair	O PCIE		
PCIE_RX2+ PCIE_RX2-	B61 B62	PCI Express channel 2, Receive Input differential pair	I PCIE		
PCIE_TX2+ PCIE_TX2-	A61 A62	PCI Express channel 2, Transmit Output differential pair	O PCIE		
PCIE_RX3+ PCIE_RX3-	B58 B59	PCI Express channel 3, Receive Input differential pair	I PCIE		
PCIE_TX3+ PCIE_TX3-	A58 A59	PCI Express channel 3, Transmit Output differential pair	O PCIE		
PCIE_RX4+ PCIE_RX4-	B55 B56	PCI Express channel 4, Receive Input differential pair	I PCIE		
PCIE_TX4+ PCIE_TX4-	A55 A56	PCI Express channel 4, Transmit Output differential pair	O PCIE		
PCIE_RX5+ PCIE_RX5-	B52 B53	PCI Express channel 5, Receive Input differential pair	I PCIE		
PCIE_TX5+ PCIE_TX5-	A52 A53	PCI Express channel 5, Transmit Output differential pair	O PCIE		
PCIE_RX6+ PCIE_RX6-	C19 C20	PCI Express channel 6, Receive Input differential pair	I PCIE		Shared with SATA port 1 (default) and configurable via the BIOS setup menu.
PCIE_TX6+ PCIE_TX6-	D19 D20	PCI Express channel 6, Transmit Output differential pair	O PCIE		
PCIE_RX7+ PCIE_RX7-	C22 C23	PCI Express channel 7, Receive Input differential pair	I PCIE		Shared with SATA port 0 (default) and configurable via the BIOS setup menu.
PCIE_TX7+ PCIE_TX7-	D22 D23	PCI Express channel 7, Transmit Output differential pair	O PCIE		
PCIE_CLK_REF+ PCIE_CLK_REF-	A88 A89	PCI Express Reference Clock output for all PCI Express and PCI Express Graphics Lanes	O PCIE		A PCI Express Gen2/3 compliant clock buffer chip must be used on the carrier board if the design involves more than one PCI Express device.

Note

SATA interface is enabled by default in BIOS setup for the shared ports.

Table 24 PCI Express Signal Descriptions (x16 Graphics)

Signal	Pin #	Description	I/O	PU/PD	Comment
PEG_RX0+ PEG_RX0-	C52 C53	PCI Express Graphics differential pairs 0 *Note: Can also be used as PCI Express differential pairs 16*	I PCIE		PCIe x8 Gen 4 ports (PEG0 - PEG7) on variants that feature the H-series processor. PCIe x4 Gen 4 ports (PEG0 - PEG4) on variants that feature the P-series and U-series processors.
PEG_TX0+ PEG_TX0-	D52 D53		O PCIE		
PEG_RX1+ PEG_RX1-	C55 C56	PCI Express Graphics differential pairs 1 *Note: Can also be used as PCI Express differential pairs 17*	I PCIE		
PEG_TX1+ PEG_TX1-	D55 D56		O PCIE		
PEG_RX2+ PEG_RX2-	C58 C59	PCI Express Graphics differential pairs 2 *Note: Can also be used as PCI Express differential pairs 18*	I PCIE		
PEG_TX2+ PEG_TX2-	D58 D59		O PCIE		
PEG_RX3+ PEG_RX3-	C61 C62	PCI Express Graphics differential pairs 3 *Note: Can also be used as PCI Express differential pairs 19*	I PCIE		
PEG_TX3+ PEG_TX3-	D61 D62		O PCIE		
PEG_RX4+ PEG_RX4-	C65 C66	PCI Express Graphics differential pairs 4 *Note: Can also be used as PCI Express differential pairs 20*	I PCIE		
PEG_TX4+ PEG_TX4-	D65 D66		O PCIE		
PEG_RX5+ PEG_RX5-	C68 C69	PCI Express Graphics differential pairs 5 *Note: Can also be used as PCI Express differential pairs 21*	I PCIE		
PEG_TX5+ PEG_TX5-	D68 D69		O PCIE		
PEG_RX6+ PEG_RX6-	C71 C72	PCI Express Graphics differential pairs 6 *Note: Can also be used as PCI Express differential pairs 22*	I PCIE		
PEG_TX6+ PEG_TX6-	D71 D72		O PCIE		
PEG_RX7+ PEG_RX7-	C74 C75	PCI Express Graphics differential pairs 7 *Note: Can also be used as PCI Express differential pairs 23*	I PCIE		
PEG_TX7+ PEG_TX7-	D74 D75		O PCIE		
PEG_RX8+ PEG_RX8-	C78 C79	PCI Express Graphics differential pairs 8 *Note: Can also be used as PCI Express differential pairs 24*	I PCIE		Not connected.
PEG_TX8+ PEG_TX8-	D78 D79		O PCIE		
PEG_RX9+ PEG_RX9-	C81 C82	PCI Express Graphics differential pairs 9 *Note: Can also be used as PCI Express differential pairs 25*	I PCIE		
PEG_TX9+ PEG_TX9-	D81 D82		O PCIE		

Signal	Pin #	Description	I/O	PU/PD	Comment
PEG_RX10+ PEG_RX10-	C85 C86	PCI Express Graphics differential pairs 10 *Note: Can also be used as PCI Express differential pairs 26*	I PCIE		Not connected.
PEG_TX10+ PEG_TX10-	D85 D86		O PCIE		
PEG_RX11+ PEG_RX11-	C88 C89	PCI Express Graphics differential pairs 11 *Note: Can also be used as PCI Express differential pairs 27*	I PCIE		
PEG_TX11+ PEG_TX11-	D88 D89		O PCIE		
PEG_RX12+ PEG_RX12-	C91 C92	PCI Express Graphics differential pairs 12 *Note: Can also be used as PCI Express differential pairs 28*	I PCIE		
PEG_TX12+ PEG_TX12-	D91 D92		O PCIE		
PEG_RX13+ PEG_RX13-	C94 C95	PCI Express Graphics differential pairs 13 *Note: Can also be used as PCI Express differential pairs 29*	I PCIE		
PEG_TX13+ PEG_TX13-	D94 D95		O PCIE		
PEG_RX14+ PEG_RX14-	C98 C99	PCI Express Graphics differential pairs 14 *Note: Can also be used as PCI Express differential pairs 30*	I PCIE		
PEG_TX14+ PEG_TX14-	D98 D99		O PCIE		
PEG_RX15+ PEG_RX15-	C101 C102	PCI Express Graphics differential pairs 15 *Note: Can also be used as PCI Express differential pairs 31*	I PCIE		
PEG_TX15+ PEG_TX15-	D101 D102		O PCIE		
PEG_LANE_RV#	D54	PCI Express Graphics lane reversal input strap. Pull low on the carrier board to reverse lane order.	I 3.3 V	PU 47.5 kΩ 3.3 V	Only for PCIe x8 reversal (H variants) and PCIe x4 reversal (P/U variants).

Note

The conga-TC675r supports PEG ports 0 - 7 (x8) on variants with H-series processor and PEG ports 0-3 (x4) on variants with P/U-series processor.

Table 25 DDI Signal Description

Signal	Pin #	Description	I/O	PU/PD	Comment
DDI1_PAIR0+ DDI1_PAIR0-	D26 D27	Multiplexed with DP1_LANE0+, TMDS1_DATA2+ and USB4_1_SSTX0+ Multiplexed with DP1_LANE0-, TMDS1_DATA2- and USB4_1_SSTX0-	O PCIE		DDI1 by default. For USB4 support, a customized BIOS is required.
DDI1_PAIR1+ DDI1_PAIR1-	D29 D30	Multiplexed with DP1_LANE1+, TMDS1_DATA1+ and USB4_1_SSRX0+ Multiplexed with DP1_LANE1-, TMDS1_DATA1- and USB4_1_SSRX0-	O PCIE		
DDI1_PAIR2+ DDI1_PAIR2-	D32 D33	Multiplexed with DP1_LANE2+, TMDS1_DATA0+ and USB4_1_SSTX1+ Multiplexed with DP1_LANE2-, TMDS1_DATA0- and USB4_1_SSTX1-	O PCIE		
DDI1_PAIR3+ DDI1_PAIR3-	D36 D37	Multiplexed with DP1_LANE3+, TMDS1_CLK+ and USB4_1_SSRX1+ Multiplexed with DP1_LANE3-, TMDS1_CLK- and USB4_1_SSRX1-	O PCIE		
SML0_CLK SML0_DAT	C25 C26	Clock line for System Management Link 0 Data line System Management Link 0	Bi-Dir OD 3.3 V	PU 499 Ω	USB4 control signals.
USB4_PD_I2C_CLK	C29	I2C clock line between module-based embedded controller master and carrier-based USB Power Delivery controller slave.	Bi-Dir OD 3.3 V	PU 2.2 kΩ 3.3 V	
USB4_PD_I2C_DAT	C30	I2C data line between module-based embedded controller master and carrier-based USB Power Delivery controller slave.	Bi-Dir OD 3.3 VSB	PU 2.2 kΩ 3.3 VSB	
USB4_1_LSTX	C15	Side band Tx interface for USB4 alternate mode	O 3.3 V	PD 1 MΩ	
USB4_1_LSRX	C16	Side bank Rx interface for USB4 alternate mode	I 3.3 V	PD 1 MΩ	
DDI1_HPD	C24	Multiplexed with DP1_HPD and HDMI1_HPD	I 3.3 V	PD 100 kΩ	
DDI1_CTRLCLK_AUX+	D15	Multiplexed with DP1_AUX+, HDMI1_CTRLCLK and USB4_1_AUX+. DP AUX+ function if DDI1_DDC_AUX_SEL is no connect. HDMI/DVI I2C CTRLCLK if DDI1_DDC_AUX_SEL is pulled high.	 I/O PCIE I/O OD 3.3 V	PD 100 kΩ	
DDI1_CTRLDATA_AUX-	D16	Multiplexed with DP1_AUX-, HDMI1_CTRLDATA and USB4_1_AUX-. DP AUX- function if DDI1_DDC_AUX_SEL is no connect. HDMI/DVI I2C CTRLDATA if DDI1_DDC_AUX_SEL is pulled high.	 I/O PCIE I/O OD 3.3 V	PU 100 kΩ 3.3 V	
DDI1_DDC_AUX_SEL	D34	Selects the function of DDI1_CTRLCLK_AUX+ and DDI1_CTRLDATA_AUX-. This pin shall have a 1 M pull-down to logic ground on the module. If this input is floating, the AUX pair is used for the DP AUX+/- signals. If pulled-high, the AUX pair contains the CTRLCLK and CTRLDATA signals.	I 3.3 V	PD 1 MΩ	
DDI2_PAIR0+ DDI2_PAIR0-	D39 D40	Multiplexed with DP2_LANE0+, TMDS2_DATA2+ and USB4_2_SSTX0+ Multiplexed with DP2_LANE0-, TMDS2_DATA2- and USB4_2_SSTX0-	O PCIE		DDI2 by default. For USB4 support, a customized BIOS is required.
DDI2_PAIR1+ DDI2_PAIR1-	D42 D43	Multiplexed with DP2_LANE1+, TMDS2_DATA1+ and USB4_2_SSRX0+ Multiplexed with DP2_LANE1-, TMDS2_DATA1- and USB4_2_SSRX0-	O PCIE		
DDI2_PAIR2+ DDI2_PAIR2-	D46 D47	Multiplexed with DP2_LANE2+, TMDS2_DATA0+ and USB4_2_SSTX1+ Multiplexed with DP2_LANE2-, TMDS2_DATA0- and USB4_2_SSTX1-	O PCIE		
DDI2_PAIR3+ DDI2_PAIR3-	D49 D50	Multiplexed with DP2_LANE3+, TMDS2_CLK+ and USB4_2_SSRX1+ Multiplexed with DP2_LANE3-, TMDS2_CLK- and USB4_2_SSRX0-	O PCIE		
DDI2_HPD	D44	Multiplexed with DP2_HPD and HDMI2_HPD	I 3.3 V	PD 100 kΩ	
DDI2_CTRLCLK_AUX+	C32	Multiplexed with DP2_AUX+, HDMI2_CTRLCLK and USB4_2_AUX+ DP AUX+ function if DDI2_DDC_AUX_SEL is no connect. HDMI/DVI I2C CTRLCLK if DDI2_DDC_AUX_SEL is pulled high	 I/O PCIE I/O OD 3.3 V	PD 100 kΩ	

Signal	Pin #	Description	I/O	PU/PD	Comment
DDI2_CTRLDATA_AUX-	C33	Multiplexed with DP2_AUX-, HDMI2_CTRLDATA and USB4_2_AUX- DP AUX- function if DDI2_DDC_AUX_SEL is no connect. HDMI/DVI I2C CTRLDATA if DDI2_DDC_AUX_SEL is pulled high.	I/O PCIE I/O OD 3.3 V	PU 100 kΩ 3.3 V	
DDI2_DDC_AUX_SEL	C34	Selects the function of DDI2_CTRLCLK_AUX+ and DDI2_CTRLDATA_AUX-. This pin shall have a 1 M pull-down to logic ground on the module. If this input is floating, the AUX pair is used for the DP AUX+/- signals. If pulled-high, the AUX pair contains the CTRLCLK and CTRLDATA signals.	I 3.3V	PD 1 MΩ	
DDI3_PAIR0+ DDI3_PAIR0-	C39 C40	Multiplexed with DP3_LANE0+ and TMDS3_DATA2+ Multiplexed with DP3_LANE0- and TMDS3_DATA2-	O PCIE		
DDI3_PAIR1+ DDI3_PAIR1-	C42 C43	Multiplexed with DP3_LANE1+ and TMDS3_DATA1+ Multiplexed with DP3_LANE1- and TMDS3_DATA1-	O PCIE		
DDI3_PAIR2+ DDI3_PAIR2-	C46 C47	Multiplexed with DP3_LANE2+ and TMDS3_DATA0+ Multiplexed with DP3_LANE2- and TMDS3_DATA0-	O PCIE		
DDI3_PAIR3+ DDI3_PAIR3-	C49 C50	Multiplexed with DP3_LANE3+ and TMDS3_CLK+ Multiplexed with DP3_LANE3- and TMDS3_CLK-	O PCIE		
DDI3_HPD	C44	Multiplexed with DP3_HPD and HDMI3	I 3.3 V	PD 100 kΩ	
DDI3_CTRLCLK_AUX+	C36	Multiplexed with DP3_AUX+ and HDMI3_CTRLCLK. DP AUX+ function if DDI3_DDC_AUX_SEL is no connect. HDMI/DVI I2C CTRLCLK if DDI3_DDC_AUX_SEL is pulled high.	I/O PCIE I/O OD 3.3 V	PD 100 kΩ	
DDI3_CTRLDATA_AUX-	C37	Multiplexed with DP3_AUX- and HDMI3_CTRLDATA. DP AUX- function if DDI3_DDC_AUX_SEL is no connect. HDMI/DVI I2C CTRLDATA if DDI3_DDC_AUX_SEL is pulled high.	I/O PCIE I/O OD 3.3 V	PU 100 kΩ 3.3 V	
DDI3_DDC_AUX_SEL	C38	Selects the function of DDI3_CTRLCLK_AUX+ and DDI3_CTRLDATA_AUX-. This pin shall have a 1 M pull-down to logic ground on the module. If this input is floating, the AUX pair is used for the DP AUX+/- signals. If pulled-high, the AUX pair contains the CTRLCLK and CTRLDATA signals.	I 3.3 V	PD 1 MΩ	

Table 26 Embedded DisplayPort Signal Descriptions

Signal	Pin #	Description	I/O	PU/PD	Comment
eDP_TX3+ eDP_TX3- eDP_TX2+ eDP_TX2- eDP_TX1+ eDP_TX1- eDP_TX0+ eDP_TX0-	A81 A82 A71 A72 A73 A74 A75 A76	eDP differential pairs	AC coupled off module.		
eDP_VDD_EN	A77	eDP power enable	O 3.3 V		
eDP_BKLT_EN	B79	eDP backlight enable	O 3.3 V		
eDP_BKLT_CTRL	B83	eDP backlight brightness control	O 3.3 V		
eDP_AUX+	A83	eDP AUX+	AC coupled off module		
eDP_AUX-	A84	eDP AUX-	AC coupled off module		
eDP_HPD	A87	Detection of hot plug / unplug and notification of the link layer	I 3.3 V	PD 100 kΩ	

Note

1. *The eDP interface is multiplexed with LVDS interface.*
2. *This interface is configured in the BIOS to support LVDS by default. For eDP support, go to Advanced -> Graphics -> Active LFP Configuration in the BIOS setup menu and select "eDP".*
3. *The LVDS/eDP interface does not support both LVDS and eDP signals at the same time.*

Table 27 LVDS Signal Descriptions

Signal	Pin #	Description	I/O	PU/PD	Comment
LVDS_A0+ LVDS_A0- LVDS_A1+ LVDS_A1- LVDS_A2+ LVDS_A2- LVDS_A3+ LVDS_A3-	A71 A72 A73 A74 A75 A76 A78 A79	LVDS Channel A differential pairs	O LVDS		
LVDS_A_CK+ LVDS_A_CK-	A81 A82	LVDS Channel A differential clock	O LVDS		
LVDS_B0+ LVDS_B0- LVDS_B1+ LVDS_B1- LVDS_B2+ LVDS_B2- LVDS_B3+ LVDS_B3-	B71 B72 B73 B74 B75 B76 B77 B78	LVDS Channel B differential pairs	O LVDS		
LVDS_B_CK+ LVDS_B_CK-	B81 B82	LVDS Channel B differential clock	O LVDS		
LVDS_VDD_EN	A77	LVDS panel power enable	O 3.3 V		
LVDS_BKLT_EN	B79	LVDS panel backlight enable	O 3.3 V		
LVDS_BKLT_CTRL	B83	LVDS panel backlight brightness control	O 3.3 V		
LVDS_I2C_CK	A83	DDC lines used for flat panel detection and control	I/O 3.3 V	PU 2.2 kΩ 3.3 V	PU for LVDS support (default).
LVDS_I2C_DAT	A84	DDC lines used for flat panel detection and control	I/O 3.3 V	PU 2.2 kΩ 3.3 V	PU for LVDS support (default).

Table 28 VGA Signal Descriptions

Signal	Pin #	Description	I/O	PU/PD	Comment
VGA_RED	B89	Red for monitor; analog DAC output designed to drive a 37.5-Ohm equivalent load	O Analog	PD 150R	Not available by default
VGA_GRN	B91	Green for monitor; analog DAC output designed to drive a 37.5-Ohm equivalent load	O Analog	PD 150R	
VGA_BLU	B92	Blue for monitor. Analog DAC output, designed to drive a 37.5-Ohm equivalent load	O Analog	PD 150R	
VGA_HSYNC	B93	Horizontal sync output to VGA monitor	O 3.3 V		

Signal	Pin #	Description	I/O	PU/PD	Comment
VGA_VSYNC	B94	Vertical sync output to VGA monitor	O 3.3 V		Not available by default
VGA_I2C_CK	B95	DDC clock line (I²C port dedicated to identify VGA monitor capabilities)	I/O OD 5 V	PU 2.2 kΩ 3.3 V	
VGA_I2C_DAT	B96	DDC data line	I/O OD 5 V	PU 2.2 kΩ 3.3 V	

Note

For VGA support, you need a customized conga-TC675r variant (assembly option).

Table 29 SATA Signal Descriptions

Signal	Pin #	Description	I/O	PU/PD	Comment
SATA0_RX+ SATA0_RX-	A19 A20	SATA channel 0, receive input differential pair	I SATA		Shared with PCIe lane 7 and configurable via the BIOS setup menu.
SATA0_TX+ SATA0_TX-	A16 A17	SATA channel 0, transmit output differential pair	O SATA		
SATA1_RX+ SATA1_RX-	B19 B20	SATA channel 1, receive input differential pair	I SATA		Shared with PCIe lane 6 and configurable via the BIOS setup menu.
SATA1_TX+ SATA1_TX-	B16 B17	SATA channel 1, transmit output differential pair	O SATA		
SATA2_RX+ SATA2_RX-	A25 A26	SATA channel 2, receive input differential pair	I SATA		Not connected.
SATA2_TX+ SATA2_TX-	A22 A23	SATA channel 2, transmit output differential pair	O SATA		
SATA3_RX+ SATA3_RX-	B25 B26	SATA channel 3, receive input differential pair	I SATA		Not connected.
SATA3_TX+ SATA3_TX-	B22 B23	SATA channel 3, transmit output differential pair	O SATA		
(S)ATA_ACT#	A28	SATA activity indicator, active low	O 3.3 V		Shared with SPKR (pin B32). Both signals are not supported at the same time.

Note

The shared signals support SATA by default.

Table 30 USB 3.x Signal Descriptions

Signal	Pin #	Description	I/O	PU/PD	Comment
USB0+	A46	USB Port 0, data + or D+	I/O		
USB0-	A45	USB Port 0, data - or D-	I/O		
USB1+	B46	USB Port 1, data + or D+	I/O		
USB1-	B45	USB Port 1, data - or D-	I/O		
USB2+	A43	USB Port 2, data + or D+	I/O		
USB2-	A42	USB Port 2, data - or D-	I/O		
USB3+	B43	USB Port 3, data + or D+	I/O		
USB3-	B42	USB Port 3, data - or D-	I/O		
USB4+	A40	USB Port 4, data + or D+	I/O		
USB4-	A39	USB Port 4, data - or D-	I/O		
USB5+	B40	USB Port 5, data + or D+	I/O		
USB5-	B39	USB Port 5, data - or D-	I/O		
USB6+	A37	USB Port 6, data + or D+	I/O		
USB6-	A36	USB Port 6, data - or D-	I/O		
USB7+	B37	USB Port 7, data + or D+	I/O		
USB7-	B36	USB Port 7, data - or D-	I/O		
USB_SSRX0+	C4	Additional receive signal differential pairs for the Superspeed USB data path	I USB_SS		
USB_SSRX0-	C3				
USB_SSTX0+	D4	Additional transmit signal differential pairs for the Superspeed USB data path	O USB_SS		
USB_SSTX0-	D3				
USB_SSRX1+	C7	Additional receive signal differential pairs for the Superspeed USB data path	I USB_SS		
USB_SSRX1-	C6				
USB_SSTX1+	D7	Additional transmit signal differential pairs for the Superspeed USB data path	O USB_SS		
USB_SSTX1-	D6				
USB_SSRX2+	C10	Additional receive signal differential pairs for the Superspeed USB data path	I USB_SS		
USB_SSRX2-	C9				
USB_SSTX2+	D10	Additional transmit signal differential pairs for the Superspeed USB data path	O USB_SS		
USB_SSTX2-	D9				
USB_SSRX3+	C13	Additional receive signal differential pairs for the Superspeed USB data path	I USB_SS		
USB_SSRX3-	C12				
USB_SSTX3+	D13	Additional transmit signal differential pairs for the Superspeed USB data path	O USB_SS		
USB_SSTX3-	D12				
USB_0_1_OC#	B44	USB over-current sense, USB ports 0 and 1. A pull-up for this line is present on the module. An open drain driver from a USB current monitor on the carrier board may drive this line low.	I 3.3 VSB	PU 10 kΩ 3.3 VSB	Do not pull this pin high on the carrier board.
USB_2_3_OC# [1]	A44	USB over-current sense, USB ports 2 and 3. A pull-up for this line is on the module. An open drain driver from a USB current monitor on the carrier board may drive this line low. .	I 3.3 VSB	PU 10 kΩ 3.3 VSB	Do not pull this pin high on the carrier board.

Signal	Pin #	Description	I/O	PU/PD	Comment
USB_4_5_OC# [1]	B38	USB over-current sense, USB ports 4 and 5. A pull-up for this line shall be present on the module. An open drain driver from a USB current monitor on the carrier board may drive this line low.	I 3.3 VSB	PU 10 kΩ 3.3 VSB	Do not pull this line high on the carrier board.
USB_6_7_OC#	A38	USB over-current sense, USB ports 6 and 7. A pull-up for this line shall be present on the module. An open drain driver from a USB current monitor on the carrier board may drive this line low.	I 3.3 VSB	PU 10 kΩ 3.3 VSB	Do not pull this line high on the carrier board.
USB0_HOST_PRSNT	B48	Module USB client may detect the presence of a USB host on USB0. A high values indicates that a host is present.	I 3.3 V	PD 47 kΩ	Not supported.
RSMRST_OUT#	A48	USB devices that are to be powered in the S5 / S4 / S3 suspend states should not have their 5V VBUS power enabled before RSMRST_OUT# transitions to the high state.	O 3.3 VSB	PD 10 kΩ	

Note

1. *USB_2_3_OC# and USB_4_5_OC# signals are connected to the same CPU overcurrent detection input.*

Table 31 USB4 Support Signal Descriptions

Signal	Pin #	Description	I/O	PU/PD	Comment
USB4_1_SSTX0+	D26	High speed USB4 port 1, data transmit pairs 0. Pins are shared with DDI1_PAIR0+ and DDI1_PAIR0-	USB_SS		DDI1 by default. For USB4 support, a customized BIOS is required.
USB4_1_SSTX0-	D27				
USB4_1_SSRX0+	D29	High speed USB4 port 1, data receive pairs 0. Pins are shared with DDI1_PAIR1+ and DDI1_PAIR1-. For 4-lane DP Alternate Mode, these RX lines are repurposed as DP TX lines per the USB4 specification.	USB_SS		
USB4_1_SSRX0-	D30				
USB4_1_SSTX1+	D32	High speed USB4 port 1, data transmit pairs 1. Pins are shared with DDI1_PAIR2+ and DDI1_PAIR2-	USB_SS		
USB4_1_SSTX1-	D33				
USB4_1_SSRX1+	D36	High speed USB4 port 1 data receive pairs 1. Pins are shared with DDI1_PAIR3+ and DDI1_PAIR3-. For 4-lane DP Alternate Mode, these RX lines are repurposed as DP TX lines per the USB4 specification.	USB_SS		
USB4_1_SSRX1-	D37				
SML0_CLK	C25	Clock lines for System Management Links 0. Pin is shared with DDI1_PAIR4+. SML0 is used to support carrier USB4 re-timers.	Bi-Dir OD 3.3 VSB	PU 499 3.3 VSB	
SML0_DAT	C26	Data line for I2C data based System Management Links between chipset masters and carrier. Pin is shared with DDI1_PAIR4-. SML0 is used to control the carrier based USB re-timers.	Bi-Dir OD 3.3 VSB	PU 499 3.3 VSB	
USB4_PD_I2C_CLK	C29	I2C clock line between module based Embedded Controller master and carrier based USB Power Delivery Controller slave. Pin is shared with DDI1_PAIR5+.	Bi-Dir OD 3.3 V	PU 2.2 KΩ 3.3 VSB	

USB4_PD_I2C_ DAT	C30	I2C data line between module based Embedded Controller master and carrier based USB Power Delivery Controller slave. Pin is shared with DDI1_PAIR5-.	Bi-Dir OD 3.3 VSB	PU 2.2 kΩ 3.3 VSB	
USB4_1_LSTX	C15	Sideband TX interface for USB4 port 1 alternate mode “Low Speed” asynchronous serial TX line. Pin is shared with DDI1_PAIR5+.	O 3.3 V	PD 1 MΩ	
USB4_1_LSRX	C16	Sideband RX interface for USB4 port 1 alternate mode “Low Speed” asynchronous serial RX line. Pin is shared with DDI1_PAIR5-.	I 3.3 V	PD 1 MΩ	
SML1_CLK	C27	Clock lines for System Management Links 1. SML1 is used to support carrier USB Power Delivery (PD) controller	Bi-Dir OD 3.3 VSB	PU 1 kΩ 3.3 VSB	
USB1_AUX+ USB1_AUX-	D15 D16	DisplayPort Aux channel for USB4 port 1 DP mode. Pins are shared with DDI_CTRLCLK_AUX+ and DDI_CTRLDATA_AUX-.	Bi-Dir LV_DIFF		
USB4_2_SSTX0+	D39	High speed USB4 port 2, data transmit pairs 0. Pins are shared with DDI2_PAIR0+ and DDI2_PAIR0-	USB_SS		DDI2 by default. For USB4 support, a customized BIOS is required.
USB4_2_SSTX0-	D40				
USB4_2_SSRX0+	D42	High speed USB4 port 2, data receive pairs 0. Pins are shared with DDI2_PAIR1+ and DDI2_PAIR1-. For 4-lane DP Alternate Mode, these RX lines are repurposed as DP TX lines per the USB4 specification.	USB_SS		
USB4_2_SSRX0-	D43				
USB4_2_SSTX1+	D46	High speed USB4 port 2, data transmit pairs 1. Pins are shared with DDI2_PAIR2+ and DDI2_PAIR2-	USB_SS		
USB4_2_SSTX1-	D47				
USB4_2_SSRX1+	D49	High speed USB4 port 2, data receive pairs 1. Pins are shared with DDI2_PAIR3+ and DDI2_PAIR3-. For 4-lane DP Alternate Mode, these RX lines are repurposed as DP TX lines per the USB4 specification.	USB_SS		
USB4_2_SSRX1-	D50				
USB2_AUX+ USB2_AUX-	C32 C33	DisplayPort Aux channel for USB4 port 2 DP mode. Pins are shared with DDI2_CTRLCLK_AUX+ and DDI2_CTRLDATA_AUX-.	Bi-Dir LV_DIFF		
USB4_2_LSTX	C35	Sideband TX interface for USB4 port 2 alternate mode “Low Speed” asynchronous serial TX line	O 3.3 V		
USB4_2_LSRX	D35	Sideband RX interface for USB4 port 2 alternate mode “Low Speed” asynchronous serial RX line	I 3.3 V		
USB4_RT_ENA	C17	Power Enable for carrier based USB Retimers. Sourced from chipset GPO “USB Re-Timer Enable”	O 3.3 V		
USB4_PD_I2C_ ALERT#	D17	Active low alert signal from USB Power Delivery controller to the module Embedded Controller	I 3.3 VSB	PU 10 kΩ 3.3 VSB	
SML1_DAT	C28	Data line for I2C data based System Management Links between chipset masters and carrier. SML1 controls the carrier based USB Power Delivery controller.	Bi-Dir OD 3.3 VSB	PU 1 kΩ 3.3 VSB	
PMCALERT#	D18	Active low alert signal associated with the SML1 System Management link, from the carrier based USB Power Delivery controller	I 3.3 VSB	PU 10 KΩ 3.3 VSB	

Note

DDI1 is shared with USB4 port 1 and DDI2 is shared with USB4 port 2. For USB4 support, a customized BIOS is required.

Table 32 NBASE-T Ethernet Signal Descriptions

Gigabit Ethernet	Pin #	Description				I/O	PU/PD	Comment
GBE0_MDI0+ GBE0_MDI0- GBE0_MDI1+ GBE0_MDI1- GBE0_MDI2+ GBE0_MDI2- GBE0_MDI3+ GBE0_MDI3-	A13 A12 A10 A9 A7 A6 A3 A2	Gigabit Ethernet Controller 0: Media Dependent Interface Differential Pairs 0, 1, 2, 3. The MDI can operate in 1000, 100, and 10 Mb/s modes or in 2.5 Gbps modes. Some pairs are unused in some modes according to the following:				I/O Analog		
			1000BASE-T 2.5GBASE-T	100BASE-TX	10BASE-T			
		MDI[0]+/-	B1_DA+/-	TX+/-	TX+/-			
		MDI[1]+/-	B1_DB+/-	RX+/-	RX+/-			
		MDI[2]+/-	B1_DC+/-					
		MDI[3]+/-	B1_DD+/-					
GBE0_ACT#	B2	Gigabit Ethernet Controller 0 activity indicator, active low				OD 3.3 VSB		
GBE0_LINK# [1, 2]	A8	Gigabit Ethernet Controller 0 link indicator, active low				OD 3.3 VSB		
GBE0_LINK_MID#	A4	Gigabit Ethernet Controller MID Speed Link indicator, active low (GBE0_LINK100# in COM Express® rev. 3.1). If active, the link is established but at a speed lower than the maximum speed supported by the Ethernet controller. Based on capabilities of the Ethernet controller used, this signal might not be active for all possible lower link speeds.				OD 3.3 VSB	PD 1 MΩ	
GBE0_LINK_MAX#	A5	Gigabit Ethernet Controller MAX Speed Link Indicator, active low (GBE0_LINK1000# in COM Express® rev 3.1). If active, the link is established at the maximum link speed supported by the controller				OD 3.3 VSB	PD 1 MΩ	
GBE0_CTREF	A14	Reference voltage for carrier board Ethernet channel 0 magnetics center tap. The reference voltage is determined by the requirements of the module PHY and may be as low as 0 V and as high as 3.3 V. The reference voltage output shall be current limited on the module. In the case in which the reference is shorted to ground, the current shall be limited to 250 mA or less.				REF		Not connected.
GBE0_SDP	A49	Gigabit Ethernet Controller 0 Software-Definable Pin. Can also be used for IEEE1588 support such as a 1 pps signal.				I/O 3.3 VSB		Signal is provided by the Intel i226-IT controller.

Note

1. *The GBE0_LINK# output is not active during a 10 Mb and 100 Mb connection. It is only active during a 1 Gb or 2.5 Gb connection. This is a limitation of Ethernet controller since it has only three LED outputs.*

2. *The GBE0_LINK# signal is a logic AND of the GBE0_LINK_MID# and GBE0_LINK_MAX# signals on the conga-TC675r module.*

Table 33 High Definition Audio Link Signals Descriptions

Signal	Pin #	Description	I/O	PU/PD	Comment
HDA_RST#	A30	Reset output to codec; active low	O 3.3 V		
HDA_SYNC	A29	Sample-synchronization signal to the codec(s)	O 3.3 V		
HDA_BITCLK	A32	Serial data clock generated by the external codec(s)	O 3.3 V		
HDA_SDOUT	A33	Serial TDM data output to the codec	O 3.3 V	PD 100 kΩ	
HDA_SDIN0	B30	Serial TDM data input from codec 0	I/O 3.3 V		
HDA_SDIN1/ SNDW0_DAT [1]	B29	Serial TDM data input from codec 1	I/O 3.3 V		
		Alternative use as Soundwire bi-directional data line	I/O 1.8 V		Not supported by default.
HDA_SDIN2/ SNDW0_CLK [1]	B28	Serial TDM data input from codec 2	I/O 3.3 V		Not supported.
		Alternative use as Soundwire bi-directional clock line	I/O 1.8 V		Not supported by default.

Note

1. *For Soundwire support, you need a customized BIOS and a customized conga-TC675r (assembly option)*

Table 34 LPC Signal Descriptions

Signal	Pin #	Description	I/O	PU/PD	Comment
LPC_AD[0:3]	B4-B7	LPC Mode: LPC multiplexed address, command and data bus	I/O 3.3 V	PU 20 kΩ 3.3 V	
LPC_FRAME#	B3	LPC Mode: LPC Frame indicates the start of a LPC cycle	O 3.3 V		
LPC_CLK	B10	LPC Mode: LPC clock output, 24 MHz	O 3.3 V		
LPC_DRQ0#	B8	LPC Mode: LPC serial DMA request	I 3.3 V		
LPC_DRQ1#	B9				
LPC_SERIRQ	A50	LPC Mode: LPC serial interrupt	I/O 3.3 V	PU 10 kΩ 3.3 V	
SUS_STAT#	B18	LPC Mode: Indicates imminent suspend operation. It is used to notify LPC devices that a low power state will be entered soon. LPC devices may need to preserve memory or isolate outputs during the low power state.	O 3.3 V		
ESPI_EN# [1]	B47	This signal is used by the carrier to indicate the operating mode of the LPC/eSPI bus. If left unconnected on the carrier, LPC mode (default) is selected. If pulled to GND on the carrier, eSPI mode is selected. This signal is pulled to a logic high on the module through a resistor. The carrier should only float this line or pull it low.	I		Not connected.

Note

1. *The conga-TC675r does not support eSPI mode.*

Table 35 SPI BIOS Flash Interface Signal Descriptions

Signal	Pin #	Description	I/O	PU/PD	Comment
SPI_CS#	B97	Chip select for carrier board SPI BIOS flash	O 3.3 VSB	PU 10 kΩ 3.3 VSB	
SPI_MISO	A92	Data in to module from carrier board SPI BIOS flash	I 3.3 VSB		
SPI_MOSI	A95	Data out from module to carrier board SPI BIOS flash	O 3.3 VSB	PU 4.75 kΩ 3.3 VSB	
SPI_CLK	A94	Clock from module to carrier board SPI BIOS flash	O 3.3 VSB		
SPI_POWER	A91	Power source for carrier board SPI BIOS flash. SPI_POWER shall be used to power SPI BIOS flash on the carrier only.	3.3 VSB		
BIOS_DIS0#	A34	Selection strap to determine the BIOS boot device	I 3.3 VSB	PU 10 kΩ 3.3 VSB	
BIOS_DIS1#	B88	Selection strap to determine the BIOS boot device. Refer to table 4.15 of the COM Express® Module Base Specification 3.1 for strapping options of BIOS disable signals.	I 3.3 VSB	PU 10 kΩ 3.3 VSB	

Table 36 Miscellaneous Signal Descriptions

Signal	Pin #	Description	I/O	PU/PD	Comment
I2C_CK	B33	General purpose I²C port clock output/input	I/O OD 3.3 VSB	PU 2.2 kΩ 3.3 VSB	
I2C_DAT	B34	General purpose I²C port data I/O line	I/O 3.3 V	PU 2.2 kΩ 3.3 VSB	
SPKR	B32	Output for audio enunciator, the "speaker" in PC-AT systems	O 3.3 V		Shared with SATA_ACT# (pin A28). Both signals are not supported at the same time.
WDT	B27	Output indicating that a watchdog time-out event has occurred	O 3.3 V	PD 100 kΩ	
FAN_PWMOUT [1]	B101	Fan speed control. Uses the Pulse Width Modulation (PWM) technique to control the fan's RPM.	O OD 3.3 V		
FAN_TACHIN [1]	B102	Fan tachometer input	I OD	PU 47.5 kΩ 3.3 V	Requires a fan with a two pulse output.
TPM_PP	A96	Physical Presence pin of Trusted Platform Module (TPM). Active high. TPM chip has an internal pull-down. This signal is used to indicate Physical Presence to the TPM.	I 3.3 V	PD 10 kΩ	Not connected to onboard TPM by default.

Note

1. *Pins are protected on the module by a series Schottky diode.*

Table 37 General Purpose I/O Signal Descriptions

Signal	Pin #	Description	I/O	PU/PD	Comment
GPO0	A93	General purpose output pins	O 3.3 V		
GPO1	B54		O 3.3 V		
GPO2	B57		O 3.3 V		
GPO3	B63		O 3.3 V		
GPI0	A54	General purpose input pins (bidirectional signal) Pulled high internally on the module.	I 3.3 V	PU 47.5 kΩ 3.3 V	
GPI1	A63		I 3.3 V	PU 47.5 kΩ 3.3 V	
GPI2	A67		I 3.3 V	PU 47.5 kΩ 3.3 V	
GPI3	A85		I 3.3 V	PU 47.5 kΩ 3.3 V	

Note

The conga-TC675r does not support SDIO.

Table 38 Power and System Management Signal Descriptions

Signal	Pin #	Description	I/O	PU/PD	Comment
PWRBTN#	B12	Power button to bring system out of S5 (soft off), active on falling edge. Note: For proper detection, assert a pulse width of at least 16 ms.	I 3.3 VSB	PU 20 kΩ 3.3 VSB	Active in S5e state.
SYS_RESET#	B49	Reset button input. Active low input. Edge triggered. System will not be held in hardware reset while this input is kept low. Note: For proper detection, assert a pulse width of at least 16 ms.	I 3.3 VSB	PU 20 kΩ 3.3 VSB	
CB_RESET#	B50	Reset output from module to Carrier Board. Active low. Issued by module chipset and may result from a low SYS_RESET# input, a low PWR_OK input, a VCC_12V power input that falls below the minimum specification, a watchdog timeout, or may be initiated by the module software.	O 3.3 VSB	PD 100 kΩ	
PWR_OK	B24	Power OK from main power supply. A high value indicates that the power is good.	I 3.3 VSB	PU 20 kΩ 3.3 VSB	Features a protection diode to support 5 V.
SUS_STAT#	B18	Indicates imminent suspend operation; used to notify LPC devices	O 3.3 VSB		
SUS_S3#	A15	Indicates system is in Suspend to RAM state. Active-low output. An inverted copy of SUS_S3# on the carrier board (also known as "PS_ON") may be used to enable the non-standby power on a typical ATX power supply.	O 3.3 VSB	PD 100 kΩ	
SUS_S4#	A18	Indicates system is in Suspend to Disk state. Active low output.	O 3.3 VSB	PD 100 kΩ	
SUS_S5#	A24	Indicates system is in Soft Off state.	O 3.3 VSB	PD 100 kΩ	
WAKE0#	B66	PCI Express wake up signal.	I 3.3 VSB	PU 1 kΩ 3.3 VSB	
WAKE1#	B67	General purpose wake up signal. May be used to implement wake-up on PS/2 keyboard or mouse activity.	I 3.3 VSB	PU 4.75 kΩ 3.3 VSB	

Signal	Pin #	Description	I/O	PU/PD	Comment
BATLOW#	A27	Battery low input. This signal may be driven low by external circuitry to signal that the system battery is low, or may be used to signal some other external power-management event.	I 3.3 VSB	PU 10 kΩ 3.3 VSB	
LID# [1]	A103	Lid switch. Used by the ACPI operating system for a LID switch. Note: For proper detection, assert a pulse width of at least 16 ms.	I 3.3 VSB	PU 47.5 kΩ 3.3 VSB	Features a protection diode to support 5 V.
SLEEP# [1]	B103	Sleep button. Used by the ACPI operating system to bring the system to sleep state or to wake it up again. Note: For proper detection, assert a pulse width of at least 16 ms.	I 3.3 VSB	PU 47.5 kΩ 3.3 VSB	Active in S5e state. Features a protection diode to support 5 V.

Note

1. *Pins are protected on the module by a series Shottky diode.*

Table 39 Rapid Shutdown Signal Descriptions

Signal	Pin #	Description	I/O	PU/PD	Comment
RAPID_ SHUTDOWN	C67	Trigger for Rapid Shutdown. Must be driven to 5V though a <=50 ohm source impedance for ≥ 20 µs.	I 3.3 V or 5 V	PD 100 kΩ	Starts the transition to the S5e state when the interrupt was caused by the RAPID_SHUTDOWN pin.

Note

The conga-TC675r does not support Rapid Shutdown.

Table 40 Thermal Protection Signal Descriptions

Signal	Pin #	Description	I/O	PU/PD	Comment
THRM#	B35	Input from off-module temp sensor indicating an over-temp situation.	I 3.3 V	PU 10 kΩ 3.3 V	
THRMTRIP#	A35	Active low output indicating that the CPU has entered thermal shutdown.	O 3.3 V	PD 100 kΩ	

Table 41 SMBus Signal Description

Signal	Pin #	Description	I/O	PU/PD	Comment
SMB_CK	B13	System Management Bus bidirectional clock line.	I/O 3.3 VSB	PU 2.2 kΩ 3.3 VSB	
SMB_DAT	B14	System Management Bus bidirectional data line.	I/O OD 3.3 VSB	PU 2.2 kΩ 3.3 VSB	
SMB_ALERT#	B15	System Management Bus Alert – active low input can be used to generate an SMI# (System Management Interrupt) or to wake the system.	I 3.3 VSB	PU 10 kΩ 3.3 VSB	

Table 42 General Purpose Serial Interface Signal Descriptions

Signal	Pin #	Description	I/O	PU/PD	Comment
SER0_TX [1, 2]	A98	General purpose serial port transmitter	O 3.3 V	PD 47.5 kΩ	
SER1_TX [1, 2]	A101	General purpose serial port transmitter	O 3.3 V	PD 47.5 kΩ kΩ	
SER0_RX [1]	A99	General purpose serial port receiver	I 3.3 V	PU 47.5 kΩ 3.3 V	
SER1_RX [1]	A102	General purpose serial port receiver	I 3.3 V	PU 47.5 kΩ 3.3 V	

Note

1. *Pins are protected on the module by a series Schottky diode.*
2. *Pull-down resistor is required on the carrier board for proper logic level.*

Table 43 General Purpose SPI Signal Descriptions

Signal	Pin #	Description	I/O	PU/PD	Comment
GP_SPI_CS#	C45	Chip select from module's SPI master to carrier's SPI slave.	O 3.3 VSB	PU 10 kΩ 3.3 VSB	
GP_SPI_MISO	B98	Serial data into module SPI master from the carrier SPI slave ("Master In Slave Out").	I 3.3 VSB		
GP_SPI_MOSI	A86	Serial data from the module SPI master to the carrier SPI slave ("Master Out Slave In").	O 3.3 VSB		
GP_SPI_CK	B99	Clock from the module SPI master to carrier SPI slave.	O 3.3 VSB		

Table 44 Module Type Definition Signal Description

<table>
<tr><th>Signal</th><th>Pin #</th><th>Description</th><th>I/O</th><th>Comment</th></tr>
<tr><td>TYPE0#
TYPE1#
TYPE2#</td><td>C54
C57
D57</td><td>The TYPE pins indicate to the carrier board the pinout type that is implemented on the module.

The pins are tied on the module to either ground (GND) or are no-connects (NC). For pinout Type 1, these pins are don’t care (X).
<table>
<tr><th>TYPE2#</th><th>TYPE1#</th><th>TYPE0#</th><th></th></tr>
<tr><td>X
NC
NC
NC
NC
GND</td><td>X
NC
NC
GND
GND
NC</td><td>X
NC
GND
NC
GND
NC</td><td>Pinout Type 1
Pinout Type 2
Pinout Type 3 (no IDE)
Pinout Type 4 (no PCI)
Pinout Type 5 (no IDE, no PCI)
Pinout Type 6 (no IDE, no PCI)</td></tr>
</table>
The carrier board should implement combinatorial logic that monitors the module ‘TYPE’ pins and keeps power off (e.g deactivates the ATX_ON signal for an ATX power supply) if an incompatible module pin-out type is detected.

The carrier board logic may also implement a fault indicator such as an LED.</td><td>PDS</td><td>TYPE[0:2]# signals are available on all modules following the Type 2-6 Pinout standard.

The conga-TC675r is based on the COM Express® Type 6 pinout therefore the pins 0 and 1 are not connected and the pin 2 is connected to GND.</td></tr>
<tr><td>TYPE10#</td><td>A97</td><td>Dual use pin.
Indicates to the carrier board that a Type 10 module is installed.
Indicates to the carrier that a Rev. 1.0/2.0 module is installed.
<table>
<tr><th>TYPE10#</th><th></th></tr>
<tr><td>NC
PD
12V</td><td>Pinout R2.0
Pinout Type 10 pull down to ground with 4.7k resistor
Pinout R1.0</td></tr>
</table>
This pin is reclaimed from VCC_12V pool. In R1.0 modules this pin will connect to other VCC_12V pins.

In R2.0 this pin is defined as a no-connect for Types 1-6. A carrier can detect a R1.0 module by the presence of 12 V on this pin. R2.0 module Types 1-6 will no-connect this pin. Type 10 modules shall pull this pin to ground through a 4.7 kΩ resistor.</td><td>PDS</td><td>Not connected to indicate “Pinout R2.0”.</td></tr>
</table>

Table 45 Power and GND Signal Descriptions

Signal	Pin #	Description	I/O	PU/PD	Comment
VCC_12V	A104-A109 B104-B109 C104-C109 D104-D109	Primary power input: +12V nominal. All available VCC_12V pins on the connector(s) shall be used.	P		
VCC_5V_SBY	B84-B87	Standby power input: +5.0V nominal. If VCC5_SBY is used, all available VCC_5V_SBY pins on the connector(s) shall be used. Only used for standby and suspend functions. May be left unconnected if these functions are not used in the system design.	P		
VCC_RTC	A47	Real-time clock circuit-power input. Nominally +3.0V.	P		
GND	A1, A11, A21, A31, A41, A51, A57, A60, A66, A70, A80, A90, A100, A110, B1, B11, B21, B31, B41, B51, B60, B70, B80, B90, B100, B110 C1, C2, C5, C8, C11, C14, C18, C21, C31, C41, C51, C60, C63, C64, C70, C73, C76, C77, C80, C83, C84, C87, C90, C93, C96, C97, C100, C103, C110, D1, D2, D5, D8, D11, D14, D21, D24, D25, D28, D31, D38, D41, D45, D48, D51, D60, D63, D64, D67, D70, D73, D76, D77, D80, D83, D84, D87, D90, D93, D96, D97, D100, D103, D110	Ground: DC power and signal and AC signal return path. All available GND connector pins shall be used and tied to the Carrier Board GND plane.	P		

9 System Resources

9.1 I/O Address Assignment

The I/O address assignment of the conga-TC675r module is functionally identical with a standard PC/AT.

Note

The BIOS assigns PCI and PCI Express I/O resources from FFF0h downwards. Non PnP/PCI/PCI Express compliant devices must not use I/O resources in that area.

9.2 eSPI/LPC Bus

On the conga-TC675r, the PCI Express bus acts as the subtractive decoding agent. All I/O cycles that are not positively decoded are forwarded to the PCI bus. Only specified I/O ranges are forwarded to the eSPI/LPC bus. In the congatec embedded BIOS, the following I/O address ranges are sent to the eSPI/LPC bus:

Table 46 Forwarded I/O Addresses

Range	Purpose
Chip Select 0	
E00h - EFFh	Always used internally
Chip Select 1	
2Eh – 2Fh	Super I/O
4Eh – 4Fh	Super I/O
60h, 64h	
8Ch – 8Dh	Used internally by eSPI to LPC bridge
A00h – A1Fh	
E00h –EFFh	Always used internally

Note

Parts of these ranges are not available if a Super I/O is used on the carrier board. If a Super I/O is not implemented on the carrier board, then these ranges are available for customer use. If you require additional eSPI/LPC bus resources other than those mentioned above, or need more information about this subject, contact congatec technical support for assistance.

9.3 PCI Configuration Space Map

Table 47 PCI Configuration Space Map

Bus Number (hex)	Device Number (hex)	Function Number (hex)	Description
00h	00h	00h	Bridge Device - Host/PCI bridge
00h	01h	00h	PCIe Root Port (PEG60) – NVMe (optional)
00h	02h	00h	Integrated Graphics Device
00h	06h	00h	PCIe Root Port (PEG10)
00h	06h	02h	PCIe Root Port (PEG62) - Network Controller
00h	0Ah	00h	Performance Monitor
00h	14h	00h	USB 3.1 xHCI Controller
00h	14h	02h	RAM Memory Controller (shared SRAM)
00h [1]	16h	00h	Intel® Management Engine Interface 1 (Intel® ME)
00h	17h	00h	SATA Interface Controller
00h [2]	1Ch	00h	PCIe Root Port 5
00h [2]	1Ch	05h	PCIe Root Port 6
00h [2]	1Ch	06h	PCIe Root Port 7
00h [2]	1Ch	07h	PCIe Root Port 8
00h [2]	1Dh	00h	PCIe Root Port 9
00h [2]	1Dh	00h	PCIe Root Port 10
00h	1Fh	00h	Intel® eSPI Controller
00h	1Fh	03h	Intel® High Definition Audio Controller
00h	1Fh	04h	SMBus Controller
00h	1Fh	05h	SPI Flash Controller
01h [3]	00h	00h	PCIe Device connected to PEG Root Port (optional NVMe onboard)
02h	00h	00h	PCIe Device connected to PEG Root Port
03h	00h	00h	Network Controller (i226-IT Intel® Ethernet controller)
04h [3]	00h	00h	PCIe Device inserted in PCI Express Port 0
05h [3]	00h	00h	PCIe Device inserted in PCI Express Port 1
06h [3]	00h	00h	PCIe Device inserted in PCI Express Port 2
07h [3]	00h	00h	PCIe Device inserted in PCI Express Port 3
08h [3]	00h	00h	PCIe Device inserted in PCI Express Port 4
09h [3]	00h	00h	PCIe Device inserted in PCI Express Port 5

Note

Internal PCI devices not connected to the conga-TC675r are not listed.

Note

1. *In the standard configuration, the Intel Management Engine (ME) related devices are partly present or not present at all.*
2. *The PCI Express ports are visible only if a device is attached to the PCI Express slot on the carrier board.*
3. *The table represents a case when a single function PCI/PCIe device is connected to all possible slots on the carrier board. The given bus numbers will change based on actual hardware configuration.*

10 BIOS Setup Description

The BIOS setup description of the conga-TC675r can be viewed without having access to the module. However, access to the restricted area of the congatec website is required in order to download the necessary tool (CgMlfViewer) and Menu Layout File (MLF).

The MLF contains the BIOS setup description of a particular BIOS revision. The MLF can be viewed with the CgMlfViewer tool. This tool offers a search function to quickly check for supported BIOS features. It also shows where each feature can be found in the BIOS setup menu.

For more information, read the application note “AN42 - BIOS Setup Description” available at www.congatec.com.

Note

If you do not have access to the restricted area of the congatec website, contact your local congatec sales representative.

10.1 Navigating the BIOS Setup Menu

The BIOS setup menu shows the features and options supported in the congatec BIOS. To access and navigate the BIOS setup menu, press the <DEL> or <F2> key during POST. The right frame displays the key legend. Above the key legend is an area reserved for text messages. These text messages explain the options and the possible impacts when changing the selected option in the left frame.

10.2 BIOS Versions

The BIOS displays the BIOS project name and the revision code during POST, and on the main setup screen. The initial production BIOS for conga-TC675r is identified as TCROR0XX or TCROR3XX, where:

- R is the identifier for a BIOS ROM file,
- 1 is the so called feature number and
- xx is the major and minor revision number.

The binary size for TCROR0XX and TCROR3XX is 32 MB.

10.3 Updating the BIOS

BIOS updates are recommeded to correct platform issues or enhance the feature set of the module. The conga-TC675r features a congatec/AMI AptioEFI firmware on an onboard flash ROM chip. You can update the firmware with the congatec System Utility. The utility has four versions—UEFI shell, Win32 command line, Win32 GUI, and Linux version.

For more information about "Updating the BIOS" refer to the user's guide for the congatec System Utility "CGUTLm1x.pdf" on the congatec website at www.congatec.com.

Caution

We recommend to use only the UEFI shell for critical updates.

10.3.1 Update from External Flash

For instructions on how to update the BIOS from external flash, refer to the AN7_External_BIOS_Update.pdf application note on the congatec website at http://www.congatec.com.

10.4 Supported Flash Devices

The conga-TC675r supports:

- Winbond W25R256JVEIQ (32 MB)

The flash device can be used on the carrier board to support external BIOS. For more information about external BIOS support, refer to the Application Note "AN7_External_BIOS_Update.pdf" on the congatec website at http://www.congatec.com.