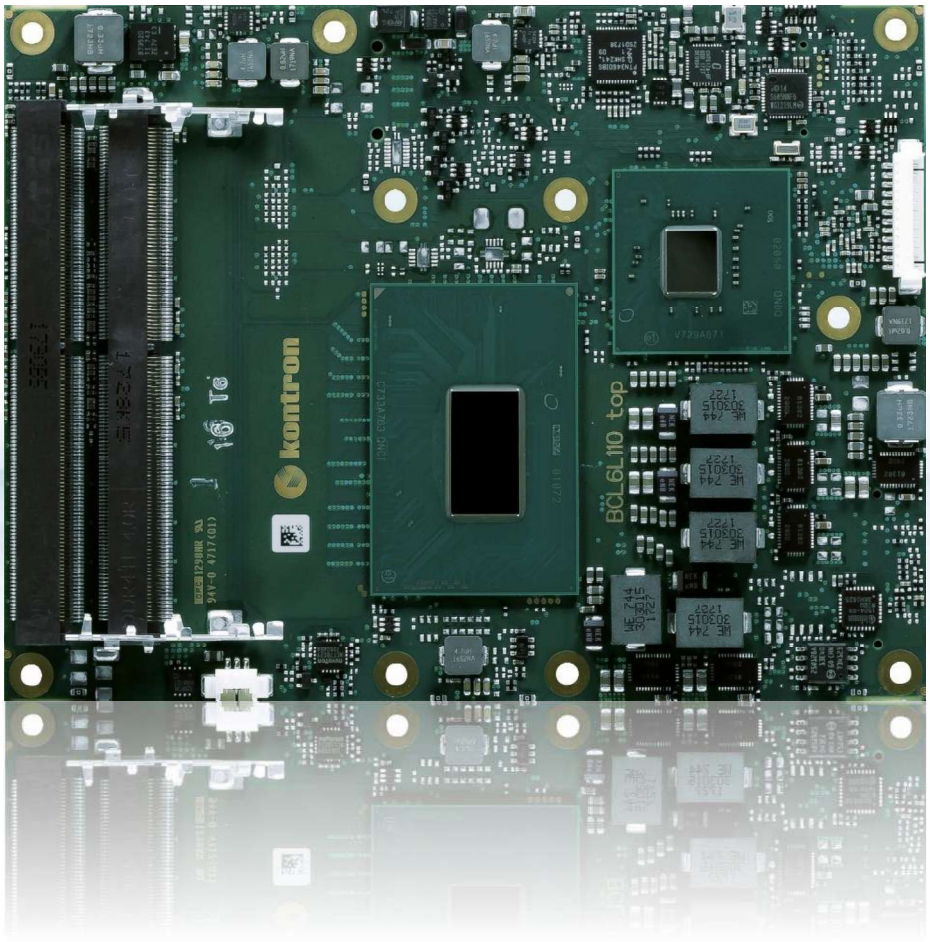
USER GUIDE



COMe-bCL6

User Guide Rev 2.6

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COME-BCL6 USER GUIDE

Disclaimer

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You understand and agree that your use of JUMPtec devices as a component in High Risk Applications is entirely at your risk. To minimize the risks associated with your products and applications, you should provide adequate design and operating safeguards. You are solely responsible for compliance with all legal, regulatory, safety, and security related requirements concerning your products. You are responsible to ensure that your systems (and any JUMPtec hardware or software components incorporated in your systems) meet all applicable requirements. Unless otherwise stated in the product documentation, the JUMPtec device is not provided with error-tolerance capabilities and cannot therefore be deemed as being engineered, manufactured or setup to be compliant for implementation or for resale as device in High Risk Applications. All application and safety related information in this document (including application descriptions, suggested safety measures, suggested JUMPtec products, and other materials) is provided for reference only.

⚠CAUTION Handling and operation of the product is permitted only for trained personnel within a work place that is access controlled. Please follow the "General Safety Instructions" supplied with the system.

NOTICE You find the most recent version of the "General Safety Instructions" online in the download area of this product.

NOTICE This product is not suited for storage or operation in corrosive environments, in particular under exposure to sulfur and chlorine and their compounds. For information on how to harden electronics and mechanics against these stress conditions, contact JUMPtec Support.

Revision History

Revision	Brief Description of Changes	Date of Issue	Author
1.0	Initial version	2018-July-30	hjs
1.1	PNs cooling accessories changed, added new processor	2018-Aug-30	hjs
1.2	MTBF, EMV test modified	2018-Dec-04	hjs
1.3	Pin A52/A53 changed, USB 3.1 Gen2 support	2019-Feb-04	hjs
1.4	BIOS Chapter screens added	2019-Apr-08	hjs
1.5	Table 2: Commercial Grade Modules (0°C to +60°C) modified	2019-Jul-30	hjs
1.6	Block diagram and variants updated, processors updated, RMA	2019-Nov-26	hjs
1.7	added chapter 3.8	2019-Dec-16	hjs
1.8	TDP i7-9850HE modified	2020-Jan-13	hjs
1.9	RTC range modified	2020-Feb-12	hjs
1.91	Chip G5600E removed	2020-Feb-25	hjs
1.92	new UL reports in Table 39, "Type 6" in chapter 3.8	2020-Jun-16	hjs
1.93	R E2S added in chapter 3.8	2020-Jul-13	hjs
1.94	Accessories change: 38116-0000-00-5	2020-Jul-22	hjs
1.95	PCH features in Table 10 corrected	2020-Oct-08	hjs
1.96	DMCM removed	2020-Dec-02	hjs
1.97	Starter Kit in Table 5 removed, new address	2020-Dec-15	hjs
1.98	Chapter "Boot problems with Xeon Modules" deleted	2021-Jan-21	hjs
1.99	Word2016 issues	2021-Mar-18	hjs
2.0	RTC Range corrected, tables in chapter 5.2 updated	2022-Jan-03	hjs
2.1	Block diagram in chapter 2.3.1: Security chip optional	2022-Feb-03	hjs
2.2	GPIO Update	2022-Jul-29	CW
2.3	Corrected Table 12 onboard fan description	2023-Oct-05	CW
2.4	Updated Ch- 5.2.3 Connector X1B Row C 1 - C 110 and CH. 5.2.4 Connector X1B Row D 1 - D 110 , signals PEG RX/TX [4:15] signals	2025-Jan-20	CW
2.5	Removed the NVME option and added new Block Diagram	2025-Sept-08	CW
2.6	Removed rapid shutdown option Removed security chip option	2025-Dec-15	IH

Terms and Conditions

JUMPtec warrants products in accordance with defined regional warranty periods. For more information about warranty compliance and conformity, and the warranty period in your region, visit http://www.congatec.com/terms-and-conditions.

JUMPtec sells products worldwide and declares regional General Terms & Conditions of Sale, and Purchase Order Terms & Conditions. Visit http://www.congatec.com/terms-and-conditions.

For contact information, refer to the corporate offices contact information on the last page of this user guide or visit our website CONTACT US.

Customer Support

Find JUMPtec contacts by visiting: https://www.JUMPtec.de/support-and-services.

Customer Service

As a trusted technology innovator and global solutions provider, JUMPtec extends its embedded market strengths into a services portfolio allowing companies to break the barriers of traditional product lifecycles. Proven product expertise coupled with collaborative and highly-experienced support enables JUMPtec to provide exceptional peace of mind to build and maintain successful products.

For more details on Kontron's service offerings such as: enhanced repair services, extended warranty, Kontron training academy, and more visit http://www.congatec.com/support-and-services/services.

Customer Comments

If you have any difficulties using this user guide, discover an error, or just want to provide some feedback, contact JUMPtec support. Detail any errors you find. We will correct the errors or problems as soon as possible and post the revised user guide on our website.

Symbols

The following symbols may be used in this user guide.

DANGER	DANGER indicates a hazardous situation which, if not avoided, will result in death or serious injury.
WARNING	WARNING indicates a hazardous situation which, if not avoided, could result in death or serious injury.
NOTICE	NOTICE indicates a property damage message.
CAUTION	CAUTION indicates a hazardous situation which, if not avoided, may result in minor or moderate injury.
	Electric Shock! This symbol and title warn of hazards due to electrical shocks (> 60 V) when touching products or parts of products. Failure to observe the precautions indicated and/or prescribed by the law may endanger your life/health and/or result in damage to your material.
	ESD Sensitive Device! This symbol and title inform that the electronic boards and their components are sensitive to static electricity. Care must therefore be taken during all handling operations and inspections of this product in order to ensure product integrity at all times.
	HOT Surface! Do NOT touch! Allow to cool before servicing.
	Laser! This symbol inform of the risk of exposure to laser beam and light emitting devices (LEDs) from an electrical device. Eye protection per manufacturer notice shall review before servicing.
	This symbol indicates general information about the product and the user guide. This symbol also indicates detail information about the specific product configuration.
	This symbol precedes helpful hints and tips for daily use.

For Your Safety

Your new JUMPtec product was developed and tested carefully to provide all features necessary to ensure its compliance with electrical safety requirements. It was also designed for a long fault-free life. However, the life expectancy of your product can be drastically reduced by improper treatment during unpacking and installation. Therefore, in the interest of your own safety and of the correct operation of your new JUMPtec product, you are requested to conform to the following guidelines.

High Voltage Safety Instructions

As a precaution and in case of danger, the power connector must be easily accessible. The power connector is the product's main disconnect device.

⚠CAUTION

Warning

All operations on this product must be carried out by sufficiently skilled personnel only.

⚠CAUTION

Electric Shock!

Before installing a non hot-swappable JUMPtec product into a system always ensure that your mains power is switched off. This also applies to the installation of piggybacks. Serious electrical shock hazards can exist during all installation, repair, and maintenance operations on this product. Therefore, always unplug the power cable and any other cables which provide external voltages before performing any work on this product.

Earth ground connection to vehicle's chassis or a central grounding point shall remain connected. The earth ground cable shall be the last cable to be disconnected or the first cable to be connected when performing installation or removal procedures on this product.

Special Handling and Unpacking Instruction

NOTICE

ESD Sensitive Device!

Electronic boards and their components are sensitive to static electricity. Therefore, care must be taken during all handling operations and inspections of this product, in order to ensure product integrity at all times.

Do not handle this product out of its protective enclosure while the product is not used for operational purposes unless the product is otherwise protected.

Whenever possible, unpack or pack this product only at EOS/ESD safe work stations. Where a safe work station is not guaranteed, it is important for the user to be electrically discharged before touching the product with his/her hands or tools. This is most easily done by touching a metal part of your system housing.

It is particularly important to observe standard anti-static precautions when changing piggybacks, ROM devices, jumper settings etc. If the product contains batteries for RTC or memory backup, ensure that the product is not placed on conductive surfaces, including anti-static plastics or sponges. They can cause short circuits and damage the batteries or conductive circuits on the product.

Lithium Battery Precautions

If your product is equipped with a lithium battery, take the following precautions when replacing the battery.

⚠CAUTION

Danger of explosion if the battery is replaced incorrectly.

- Replace only with same or equivalent battery type recommended by the manufacturer.
- Dispose of **used batteries according to the manufacturer's instructions.**

General Instructions on Usage

In order to maintain Kontron's product warranty, this product must not be altered or modified in any way. Changes or modifications to the product, that are not explicitly approved by JUMPtec and described in this user guide or received from JUMPtec Support as a special handling instruction, will void your warranty.

This product should only be installed in or connected to systems that fulfill all necessary technical and specific environmental requirements. This also applies to the operational temperature range of the specific board version that must not be exceeded. If batteries are present, their temperature restrictions must be taken into account.

In performing all necessary installation and application operations, only follow the instructions supplied by the present user guide.

Keep all the original packaging material for future storage or warranty shipments. If it is necessary to store or ship the product then re-pack it in the same manner as it was delivered.

Special care is necessary when handling or unpacking the product. See Special Handling and Unpacking Instruction.

Quality and Environmental Management

JUMPtec aims to deliver reliable high-end products designed and built for quality, and aims to complying with environmental laws, regulations, and other environmentally oriented requirements. For more information regarding Kontron's quality and environmental responsibilities, visit http://www.congatec.com/about-JUMPtec/corporate-responsibility/quality-management.

Disposal and Recycling

Kontron's products are manufactured to satisfy environmental protection requirements where possible. Many of the components used are capable of being recycled. Final disposal of this product after its service life must be accomplished in accordance with applicable country, state, or local laws or regulations.

WEEE Compliance

The Waste Electrical and Electronic Equipment (WEEE) Directive aims to:

- Reduce waste arising from electrical and electronic equipment (EEE)
- Make producers of EEE responsible for the environmental impact of their products, especially when the product become waste
- Encourage separate collection and subsequent treatment, reuse, recovery, recycling and sound environmental disposal of EEE
- Improve the environmental performance of all those involved during the lifecycle of EEE

Environmental protection is a high priority with JUMPtec

follows the WEEE directive

You are encouraged to return our products for proper disposal.

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1/ Introduction

1.1. Product Description

JUMPtec´s Computer-on-Module COMe-bCL6 is a COM Express® Basic Type 6 pinout based on the Intel® 8th/9th Generation Core ™/Xeon® processors. The COMe-bCL6 supports additional communication interfaces via a separate Chipset (CM246/QM370 PCH). Due to Intel's 14nm technology, the processor offers increased efficiency and performance with TDP as low as 25 to 45 W for quad-core chips and 25 to 45 W for six cores.

Basic COMe-bCL6 features are:

- Intel® 8th/9th Generation Core series with CM246/QM370 PCH
- Up to 4x DDR4-2666 SO-DIMM with up to 128 GByte (non-ECC/ECC) (3rd/4th socket on request)
- High-speed connectivity includes 8x PCIe x1, 1x PEG x16, 1x 1 GbE
- Support for the Industrial temperature environment

1.2. Product Naming Clarification

COM Express® defines a Computer-On-Module, or COM, with all the components necessary for a bootable host computer, packaged as a super component. The product names for JUMPtec COM Express® Computer-on-Modules consist of:

- Short form of the industry standard
  - COMe-bCL6
- Module form factor
  - b=basic (125 mm x 95 mm)
  - c=compact (9 5mm x 95 mm)
  - m=mini (84 mm x 55 mm)
- Processor code name
  - CL = Coffee Lake
- Pinout type
  - Type 6
- Temperature variants
  - Commercial
  - Extended (E1)
  - Industrial (E2)
  - Screened industrial (E2S) and Rapid shutdown screened industrial (R E2S)
- Processor Identifier
  - Chipset identifier (if chipset assembled)
- Memory size
  - Memory Down + DIMM memory (#GB)/eMMC SLC memory (#S)

1.3. COM Express® Documentation

The COM Express® Specification defines the COM Express® module form factor, pinout and signals. The COM Express document is available at the PICMG® website.

1.4. COM Express® Functionality

All JUMPtec COM Express® basic and compact modules contain two 220-pin connectors; each of which has two rows called row A & B on the primary connector and row C & D on the secondary connector. The COM Express® Computer-On-Module (COM) features the following maximum amount of interfaces according to the PCI Industrial Computer Manufacturers Group (PICMG) module pinout type.

Table 1: Pin Assignment of Type 6 and COMe-bCL6

Feature	Type 6 Pinout	COMe-bCL6 Pinout
HD Audio	1x	1x
Gb Ethernet	1x	1x
Serial ATA	4x	4x
PCI Express x 1	8x	8x
PCI Express x16 (PEG)	1x	1x
USB	4x USB 3.0 (Incl. USB 2.0) + 4x USB 2.0	4x USB 3.1 Gen 2 (Incl. USB 2.0) + 4x USB 2.0 Corresponding USB ports are configured to USB 3.1 Gen1 by default as support depends on appropriate carrier board design
VGA	1x	1x (optional)
LVDS	Dual Channel	Dual Channel LVDS with option to overlay with embedded Display port (eDP)
DP++ (eDP/DP/HDMI/DVI/VGA)	3x	3x
LPC	1x	1x
External SMB	1x	1x
External I2C	1x	1x
GPIO	8x	8x
SDIO shared w/GPIO	1x optional	
UART (2-wire COM)	2x	2x
FAN PWM out	1x	1x

1.5. COM Express® Benefits

COM Express® modules are very compact, highly integrated computers. All JUMPtec COM Express® modules feature a standardized form factor and a standardized connector layout that carry a specified set of signals. Each COM is based on the COM Express® specification. This standardization allows designers to create a single-system baseboard that can accept present and future COM Express® modules.

The baseboard designer can optimize exactly how each of these functions implements physically. Designers can place connectors precisely where needed for the application, on a baseboard optimally designed to fit a system's packaging.

A single baseboard design can use a range of COM Express® modules with different sizes and pinouts. This flexibility differentiates products at various price and performance points and provides a built-in upgrade path when designing future-proof systems. The modularity of a COM Express® solution also ensures against obsolescence when computer technology evolves. A properly designed COM Express® baseboard can work with several successive generations of COM Express® modules.

A COM Express® baseboard design has many advantages of a customized computer-board design and, additionally, delivers better obsolescence protection, heavily reduced engineering effort, and faster time to market.

2/ Product Specification

2.1. Module Variants

The COM Express® basic sized, Computer-on-Module COMe-bCL6, uses pinout Type 6 and is compatible with the PICMG specification COM.0 Rev. 3.0. The COMe-bCL6 is available in different variants to cover demands in performance, price and power.

2.1.1. Commercial Grade Modules (0°C to +60°C)

Commercial Grade Modules (0°C to +60°C) are available as a standard product number.

Table 2: Commercial Grade Modules (0°C to +60°C)

Product Number	Product Name	Comment
38034-0000-28-6	COMe-bCL6 E-2276ME CM246	COM Express® basic pin-out type 6 Computer-on-Module with Intel® Xeon® E-2276ME, 6x2.8GHz, CM246 PCH, GT2, 2x DDR4 non-ECC/ECC SO-DIMM
38034-0000-27-6	COMe-bCL6 E-2176M CM246	COM Express® basic pin-out type 6 Computer-on-Module with Intel® Xeon® E-2176M, 6x2.7GHz, CM246 PCH, GT2, 2x DDR4 non-ECC/ECC SO-DIMM
38034-0000-20-6	COMe-bCL6 E-2276ML CM246	COM Express® basic pin-out type 6 Computer-on-Module with Intel® Xeon® E-2276ML, 6x2.0GHz, CM246 PCH, GT2, 2x DDR4 non-ECC/ECC SO-DIMM
38034-0000-26-4	COMe-bCL6 E-2254ME CM246	COM Express® basic pin-out type 6 Computer-on-Module with Intel® Xeon® E-2254ME, 4x2.6GHz, CM246 PCH, GT2, 2x DDR4 non-ECC/ECC SO-DIMM
38034-0000-17-4	COMe-bCL6 E-2254ML CM246	COM Express® basic pin-out type 6 Computer-on-Module with Intel® Xeon® E-2254ML, 4x1.7GHz, CM246 PCH, GT2, 2x DDR4 non-ECC/ECC SO-DIMM
38034-0000-27-7	COMe-bCL6 i7-9850HE QM370	COM Express® basic pin-out type 6 Computer-on-Module with Intel® Core™ i7-9850HE, 6x2.7GHz, QM370 PCH, GT2, 2x DDR4 non-ECC SO-DIMM
38034-0000-26-7	COMe-bCL6 i7-8850H QM370	COM Express® basic pin-out type 6 Computer-on-Module with Intel® Core™ i7-8850H, 6x2.6GHz, QM370 PCH, GT2, 2x DDR4 non-ECC SO-DIMM
38034-0000-19-7	COMe-bCL6 i7-9850HL QM370	COM Express® basic pin-out type 6 Computer-on-Module with Intel® Core™ i7-9850HL, 6x1.9GHz, QM370 PCH, GT2, 2x DDR4 non-ECC SO-DIMM
38034-0000-25-5	COMe-bCL6 i5-8400H QM370	COM Express® basic pin-out type 6 Computer-on-Module with Intel® Core™ i5-8400H, 4x2.5GHz, QM370 PCH, GT2, 2x DDR4 non-ECC SO-DIMM
38034-0000-30-3	COMe-bCL6 i3-8100H QM370	COM Express® basic pin-out type 6 Computer-on-Module with Intel® Core™ i3-8100H, 4x3.0GHz, QM370 PCH, GT2, 2x DDR4 non-ECC SO-DIMM
38034-0000-16-3	COMe-bCL6 i3-9100HL QM370	COM Express® basic pin-out type 6 Computer-on-Module with Intel® Core™ i3-9100HL, 4x1.6GHz, QM370 PCH, GT2, 2x DDR4 non-ECC SO-DIMM
38034-0000-24-2	COMe-bCL6 G4930E QM370	COM Express® basic pin-out type 6 Computer-on-Module with Intel® Celeron® G4930E, 2x2.4GHz, QM370 PCH, GT2, 2x DDR4 non-ECC SO-DIMM

Product Number	Product Name	Comment
38034-0000-19-2	COMe-bCL6 G4932E QM370	COM Express® basic pin-out type 6 Computer-on-Module with Intel® Celeron® G4932E, 2x1.9GHz, QM370 PCH, GT2, 2x DDR4 non-ECC SO-DIMM

2.1.2. Extended Temperature Grade Modules (E1, -25 °C to +75 °C)

Extended Temperature grade modules (E1, -25°C to 75°C) are available as a standard product number, on request. For further information, contact your local JUMPtec sales representative or JUMPtec Inside Sales.

2.1.3. R E2S Modules (R E2S, -40°C to +85°C)

The following table provides a list of R E2S modules available with E2 temperature grade (-40°C to +85°C) by screening (Rapid Shutdown no longer supported as of PCN BCL6V220)

For further information regarding the screening process contact JUMPtec Support

Table 3: R E2S Modules (R E2S, -40°C to +85°C)

Product Number	Product Name	Comment
38035-0000-28-6	COMe-bCL6R E2S E-2276ME CM246	COM Express® basic pin-out type 6 Computer-on-Module with Intel® Xeon® E-2276ME, 6x2.8GHz, CM246 PCH, GT2, 2x DDR4 non-ECC/ECC SO-DIMM, industrial temperature grade
38035-0000-27-6	COMe-bCL6R E2S E-2176M CM246	COM Express® basic pin-out type 6 Computer-on-Module with Intel® Xeon® E-2176M, 6x2.7GHz, CM246 PCH, GT2, 2x DDR4 non-ECC/ECC SO-DIMM, industrial temperature grade
38035-0000-20-6	COMe-bCL6R E2S E-2276ML CM246	COM Express® basic pin-out type 6 Computer-on-Module with Intel® Xeon® E-2276ML, 6x2.0GHz, CM246 PCH, GT2, 2x DDR4 non-ECC/ECC SO-DIMM, industrial temperature grade
38035-0000-26-4	COMe-bCL6R E2S E-2254ME CM246	COM Express® basic pin-out type 6 Computer-on-Module with Intel® Xeon® E-2254ME, 4x2.6GHz, CM246 PCH, GT2, 2x DDR4 non-ECC/ECC SO-DIMM, industrial temperature grade
38035-0000-17-4	COMe-bCL6R E2S E-2254ML CM246	COM Express® basic pin-out type 6 Computer-on-Module with Intel® Xeon® E-2254ML, 4x1.7GHz, CM246 PCH, GT2, 2x DDR4 non-ECC/ECC SO-DIMM, industrial temperature grade
38035-0000-27-7	COMe-bCL6R E2S i7-9850HE QM370	COM Express® basic pin-out type 6 Computer-on-Module with Intel® Core™ i7-9850HE, 6x2.7GHz, QM370 PCH, GT2, 2x DDR4 non-ECC SO-DIMM, industrial temperature grade
38035-0000-26-7	COMe-bCL6R E2S i7-8850H QM370	COM Express® basic pin-out type 6 Computer-on-Module with Intel® Core™ i7-8850H, 6x2.6GHz, QM370 PCH, GT2, 2x DDR4 non-ECC SO-DIMM, industrial temperature grade
38035-0000-19-7	COMe-bCL6R E2S i7-9850HL QM370	COM Express® basic pin-out type 6 Computer-on-Module with Intel® Core™ i7-9850HL, 6x1.9GHz, QM370 PCH, GT2, 2x DDR4 non-ECC SO-DIMM, industrial temperature grade
38035-0000-25-5	COMe-bCL6R E2S i5-8400H QM370	COM Express® basic pin-out type 6 Computer-on-Module with Intel® Core™ i5-8400H, 4x2.5GHz, QM370 PCH, GT2, 2x DDR4 non-ECC SO-DIMM, industrial temperature grade

Product Number	Product Name	Comment
38035-0000-30-3	COMe-bCL6R E2S i3-8100H CM246	COM Express® basic pin-out type 6 Computer-on-Module with Intel® Core™ i3-8100H, 4x3.0GHz, CM246 PCH, GT2, 2x DDR4 non-ECC/ECC SO-DIMM, industrial temperature grade
38035-0000-16-3	COMe-bCL6R E2S i3-9100HL CM246	COM Express® basic pin-out type 6 Computer-on-Module with Intel® Core™ i3-9100HL, 4x1.6GHz, CM246 PCH, GT2, 2x DDR4 non-ECC/ECC SO-DIMM, industrial temperature grade
38035-0000-24-2	COMe-bCL6R E2S G4930E CM246	COM Express® basic pin-out type 6 Computer-on-Module with Intel® Celeron® G4930E, 2x2.4GHz, CM246 PCH, GT2, 2x DDR4 non-ECC/ECC SO-DIMM, industrial temperature grade
38035-0000-19-2	COMe-bCL6R E2S G4932E CM246	COM Express® basic pin-out type 6 Computer-on-Module with Intel® Celeron® G4932E, 2x1.9GHz, CM246 PCH, GT2, 2x DDR4 non-ECC SO-DIMM, industrial temperature grade

2.2. Accessories

The following tables provide a list of specific and general COMe-bCL6 accessories. For more information, contact your local JUMPtec sales representative or JUMPtec Inside Sales.

Table 4: Product Specific Accessories

Part Number	Heatspreader	Comment
38030-0000-99-0	HSP COMe-bSL6/bKL6/bCL6 Cu-core threaded	For all CPUs and temperature grades
38030-0000-99-1	HSP COMe-bSL6/bKL6/bCL6 Cu-core through	For all CPUs and temperature grades

Table 5: COMe Type 6 Specific Accessories

Part Number	COMe Carrier	Project Code	Comment
38115-0000-00-x	COM Express® Reference Carrier-i Type 6	ADTI	Thin-mITX Carrier with 5 mm COMe connector
38116-0000-00-5	COM Express® Eval Carrier2 Type 6	ADT6	ATX Carrier with 5 mm COMe connector
Part Number	COMe Adapter / Card	Project Code	Comment
96007-0000-00-3	ADA-PCIe-DP	APDP	PCIe x16 to DP Adapter for Evaluation Carrier
96007-0000-00-7	ADA-Type6-DP3	DVO6	(sandwich) Adapter Card for 3x DisplayPort
96006-0000-00-2	COMe POST T6	NFCB	POST Code / Debug Card
38019-0000-00-0	ADA-COMe-Height-dual	EERC	Height Adapter

Table 6: General Accessories

Part Number	Cooling Solutions	Comments
38025-0000-99-0C05	HSK COMe-bHL6/bBL6/bSL6/-bKL6/bCL6 active (w/o HSP)	For all CPUs and commercial temperature grade usage, to be mounted on HSP
38025-0000-99-0C06	HSK COMe-bHL6/bBL6/bSL6/-bKL6/bCL6 passive (w/o HSP)	For all CPUs and commercial temperature grade usage, to be mounted on HSP
Part Number	Mounting	Comments
38017-0000-00-5	COMe Mount KIT 5 mm 1 set	Mounting Kit for 1 module including screws for 5 mm connectors
38017-0100-00-5	COMe Mount KIT 5 mm 100 sets	Mounting Kit for 100 modules including screws for 5 mm connectors
38017-0000-00-0	COMe Mount KIT 8 mm 1 set	Mounting Kit for 1 module including screws for 8 mm connectors
38017-0100-00-0	COMe Mount KIT 8 mm 100 sets	Mounting Kit for 100 modules including screws for 8 mm connectors
Part Number	Display Adapter	Comment
96006-0000-00-8	ADA-DP-LVDS	DP to LVDS adapter
96082-0000-00-0	KAB-ADAPT-DP-DVI	DP to DVI adapter cable
96083-0000-00-0	KAB-ADAPT-DP-VGA	DP to VGA adapter cable
96084-0000-00-0	KAB-ADAPT-DP-HDMI	DP to HDMI adapter cable
Part Number	Cables	Comment
96079-0000-00-0	KAB-HSP 200mm	Cable adapter to connect FAN to module (COMe basic/compact)
96079-0000-00-2	KAB-HSP 40 mm	Cable adapter to connect FAN to module (COMe basic/compact)

Table 7: Memory Modules

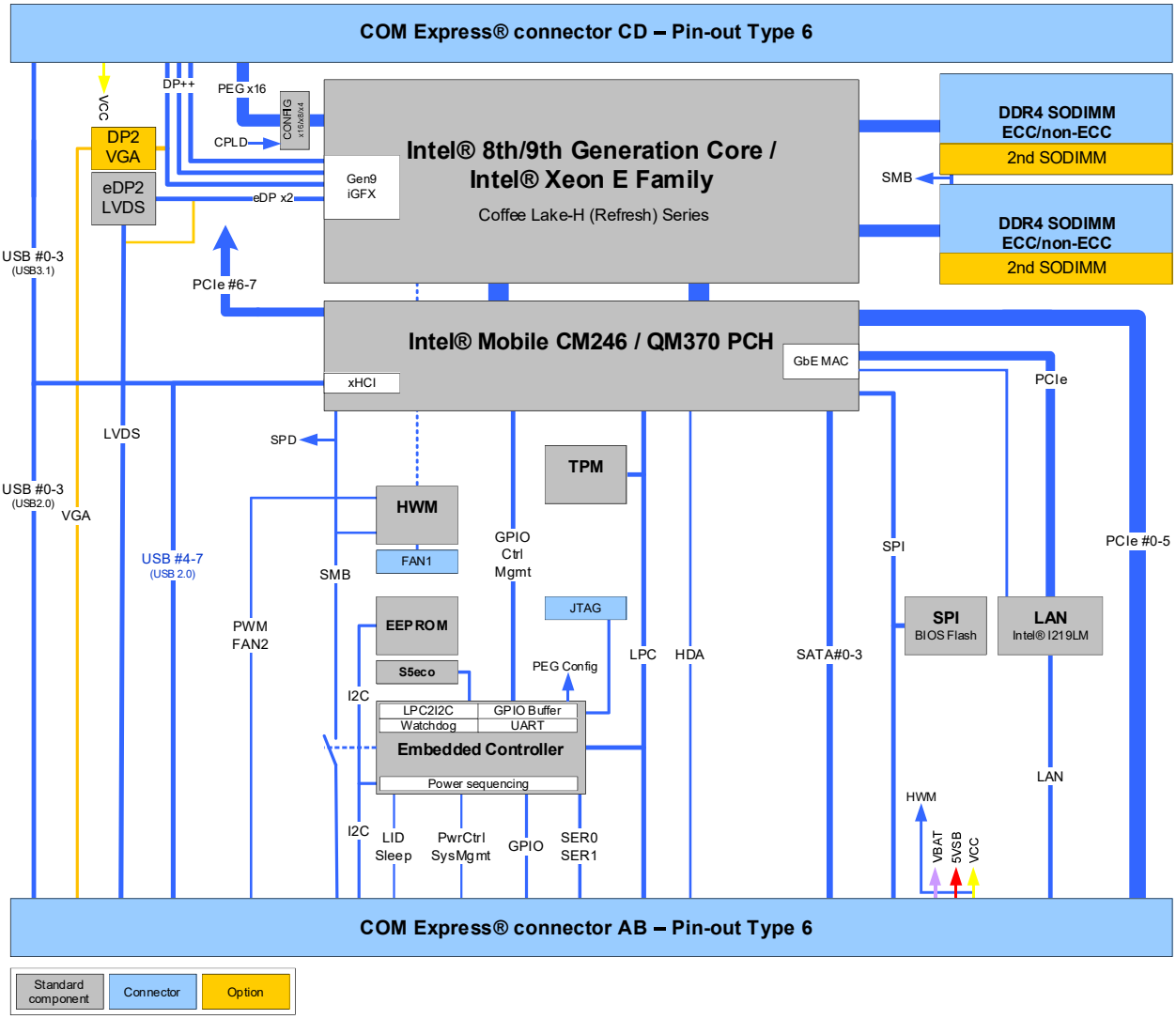
Part Number	Memory (validated reference types)	
97017-4096-27-0	DDR4-2666 SODIMM 4GB_COM	DDR4-2666, 4GB, 260P, 1333MHz, PC4-2666 SODIMM
97017-8192-27-0	DDR4-2666 SODIMM 8GB_COM	DDR4-2666, 8GB, 260P, 1333MHz, PC4-2666 SODIMM
97017-1600-27-0	DDR4-2666 SODIMM 16GB_COM	DDR4-2666, 16GB, 260P, 1333MHz, PC4-2666 SODIMM
97017-3200-27-0	DDR4-2666 SODIMM 32GB_COM	DDR4-2666, 32GB, 260P, 1333MHz, PC4-2666 SODIMM
97017-4096-27-2	DDR4-2666 SODIMM 4GB E2_COM	DDR4-2666, 4GB, E2, 260P, 1333MHz, PC4-2666 SODIMM
97017-8192-27-2	DDR4-2666 SODIMM 8GB E2_COM	DDR4-2666, 8GB, E2, 260P, 1333MHz, PC4-2666 SODIMM
97017-1600-27-2	DDR4-2666 SODIMM 16GB E2_COM	DDR4-2666, 16GB, E2, 260P, 1333MHz, PC4-2666 SODIMM
97017-3200-27-2	DDR4-2666 SODIMM 32GB E2_COM	DDR4-2666, 32GB, E2, 260P, 1333MHz, PC4-2666 SODIMM
Part Number	Memory ECC (validated reference types)	
97018-4096-27-0	DDR4-2666 SODIMM 4GB ECC_COM	DDR4-2666, 4GB, ECC, 260P, 1333MHz, PC4-2666 SODIMM
97018-8192-27-0	DDR4-2666 SODIMM 8GB ECC_COM	DDR4-2666, 8GB, ECC, 260P, 1333MHz, PC4-2666 SODIMM
97018-1600-27-0	DDR4-2666 SODIMM 16GB ECC_COM	DDR4-2666, 16GB, ECC, 260P, 1333MHz, PC4-2666 SODIMM
97018-3200-27-0	DDR4-2666 SODIMM 32GB ECC_COM	DDR4-2666, 32GB, ECC, 260P, 1333MHz, PC4-2666 SODIMM
97018-4096-27-2	DDR4-2666 SODIMM 4GB ECC E2_COM	DDR4-2666, 4GB, ECC, E2, 260P, 1333MHz, PC4-2666 SODIMM
97018-8192-27-2	DDR4-2666 SODIMM 8GB ECC E2_COM	DDR4-2666, 8GB, ECC, E2, 260P, 1333MHz, PC4-2666 SODIMM
97018-1600-27-2	DDR4-2666 SODIMM 16GB ECC E2_COM	DDR4-2666, 16GB, ECC, E2, 260P, 1333MHz, PC4-2666 SODIMM
97018-3200-27-2	DDR4-2666 SODIMM 32GB ECC E2_COM	DDR4-2666, 32GB, ECC, E2, 260P, 1333MHz, PC4-2666 SODIMM

2.3. Functional Specification

2.3.1. Block Diagram COMe-bCL6

The following figure displays the system block diagram applicable to all COMe-bCL6 modules.

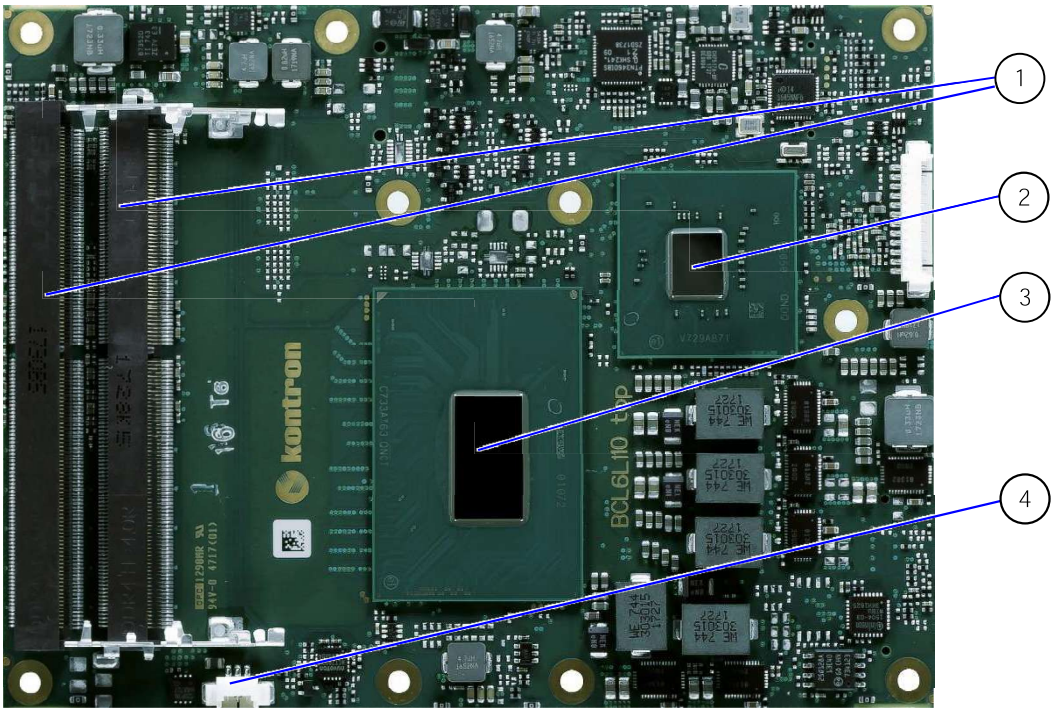
Figure 1: Block Diagram COMe-bCL6



2.3.2. Front and Bottom View

2.3.2.1. Front View

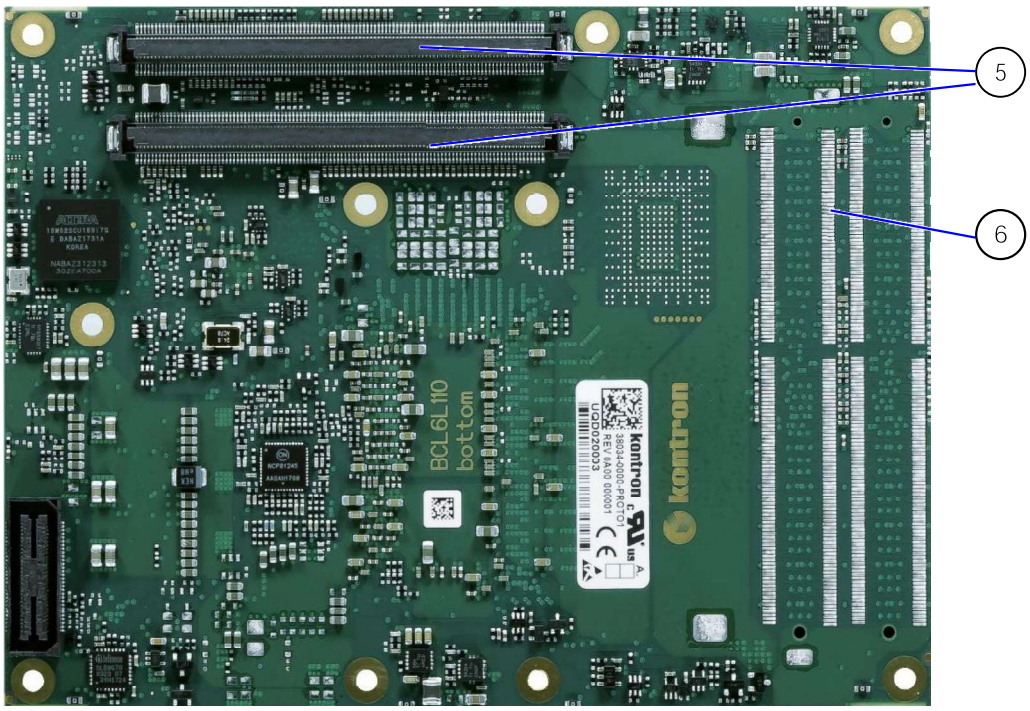
Figure 2: Front View COMe-bCL6



1. 2x SO-DIMM slots
2. PCH
3. Processor
4. Fan connector

2.3.2.2. Bottom View

Figure 3: Bottom View COMe-bCL6



5. 2x COMe interfaces X1A and X1B
6. Place for additional SO-DIMM slots

2.3.3. Technical Data

Table 8: Technical Data

Function	Definition
Compliance	COM Express® basic, Pin-out Type 6
Dimensions (H X W)	125 x 95 mm
CPU	Intel 8th/9th Generation Core/Xeon Series, Package: BGA1440: Intel® Xeon® E-2276ME/ML, Intel® Xeon® E-2254ME/ML, Intel® Core™ i7-9850HE/HL, Intel® Core™ i3-9100HL, Intel® Celeron® G4930E, Intel® Celeron® G4932E, Intel® Xeon® E-2176M, Intel® Core™ i7-8850H. Intel® Core™ i5-8400H, Intel® Core™ i3-8100H
Chipset	CM246 PCH, QM370 PCH
Main Memory	Channel 1: Up to 2x SO-DIMMs DDR4, max 32 GB per DIMM 2133/2400/2660 MHz non-ECC/ECC Channel 2: Up to 2x SO-DIMMs DDR4, max 32 GB per DIMM 2133/2400/2660 MHz non-ECC/ECC
Graphics Controller	Intel® HD Graphics (P)630, UHD 610 for Celeron®
Graphic Interfaces	3x DP, LVDS (Dual Channel 18/24bit), VGA and eDP optional
Ethernet Controller	Intel® I219LM
Ethernet	10/100/1000 MBit Ethernet
Hard Disk	4x SATA 6Gb/s
PCI Express® Support	8x PCIe x1, 1x PEG x16
USB	4x USB 3.1 (incl. USB 2.0) + 4x USB 2.0
Serial	2x serial interfaces (RX/TX Only)
Audio	Intel® High Definition Audio
Common Features	SPI, LPC, SMBus, Fast I²C, Staged Watchdog, RTC
BIOS	AMI Aptio V
Power Management	ACPI 6.0
Power Supply	8.5 V to 20 V Wide Range, Single Supply Power
Special Features	POSCAP capacitors, Trusted Platfom Module TPM 2.0, 4k Resolutions, Flexible PEG Lane Configuration by Setup Option
Operating System	Windows® 10, Linux, VxWorks
Temperature	Commercial Grade Temperature: -0 °C to +60 °C operating, -30 °C to +85 °C non-operating Extended Temperature: -25 °C to +75 °C operating, -30 °C to +85 °C non-operating Industrial Temperature: -40 °C To +85 °C operating, -40 °C to +85 °C non-operating

2.3.4. Processor

The Intel® 8th/9th Generation Core™ series product family uses the 14 nm process technology, with 42 mm x 28 mm package size and BG1440 socket.

In general, the processors supports the following technologies:

- Intel® Optane™ Memory Supported
- Intel® Turbo Boost Technology 2.0
- Intel® vPro™ Technology
- Intel® Hyper-Threading Technology
- Intel® Virtualization Technology (VT-x)
- Intel® Virtualization Technology for Directed I/O (VT-d)
- Intel® VT-x with Extended Page Tables (EPT)
- Intel® TSX-NI
- Intel® 64
- Instruction Set 64-bit
- Instruction Set Extensions Intel® SSE4.1, Intel® SSE4.2, Intel® AVX2
- Idle States
- Enhanced Intel SpeedStep® Technology
- Thermal Monitoring Technologies
- Intel® Identity Protection Technology

Security & Reliability

- Intel® AES New Instructions (on request)
- Secure Key
- Intel® Software Guard Extensions (Intel® SGX)
- Intel® Memory Protection Extensions (Intel® MPX)
- Intel® OS Guard
- Intel® Trusted Execution Technology
- Execute Disable Bit
- Intel® Boot Guard

Table 9: Specifications of the COMe-bCL6 Processor Variants

Processor	Cores/ Threads	Frequency nom./Turbo	L3-Cache	TDP/$T_{Junction}$	Graphics
Intel® Xeon® E-2276ME	6/12	2.8/4.5 GHz	12 MByte	45 W/100°C	UHD-Graphics P630
Intel® Xeon® E-2276ML	6/12	2.0/4.2 GHz	12 MByte	25 W/100°C	UHD-Graphics P630
Intel® Xeon® E-2254ME	4/8	2.6/3.8 GHz	8 MByte	45 W/100°C	UHD-Graphics P630
Intel® Xeon® E-2254ML	4/8	1.7/3.5 GHz	8 MByte	25 W/100°C	UHD-Graphics P630
Intel® Core™ i7-9850HE	6/12	2.7/4.4 GHz	9 MByte	45 W/100°C	UHD-Graphics 630
Intel® Core™ i7-9850HL	6/12	1.9/4.1 GHz	9 MByte	25 W/100°C	UHD-Graphics 630
Intel® Core™ i3-9100HL	4/4	1.6/2.9 GHz	6 MByte	25 W/100°C	UHD-Graphics 630
Intel® Celeron® G4930E	2/2	2.4/2.4 GHz	2 MByte	35 W/100°C	UHD-Graphics 610
Intel® Celeron® G4932E	2/2	1.9/1.9 GHz	2 MByte	25 W/100°C	UHD-Graphics 610
Intel® Xeon® E-2176M	6/12	2.7/4.4 GHz	12 MByte	45 W/100°C	UHD-Graphics P630
Intel® Core™ i7-8850H	6/12	2.6/4.3 GHz	9 MByte	45 W/100°C	UHD-Graphics 630
Intel® Core™ i5-8400H	4/8	2.5/4.2 GHz	8 MByte	45 W/100°C	UHD-Graphics 630
Intel® Core™ i3-8100H	4/4	3.0 GHz	6 MByte	45 W/100°C	UHD-Graphics 630

2.3.5. Chipset

The COMe-bCL6 is a two-chip solution implementing the H CPU and CM246, QM370 and optional HM370 Platform Controller Hub.

2.3.5.1. Platform Controller Hub (PCH)

The following table lists the PCH QM370 and CM246 PCH features.

Table 10: PCH QM370 and CM246 Features

Feature	QM370	CM246
Max USB 3.1 Gen2 (10 Gb/s)/Gen 1 (5 Gb/s)	4	4
Displays	3	3
PCIe lanes	8	8
PCIe Configurations	x1, x2, x4	x1, x2, x4
Smart Surround	yes	yes
vPRO Technology	yes	yes
TDP	3 W	3 W
ECC memory support	no	yes

2.3.6. System Memory

The COMe-bCL6 supports a dual DDR4 memory interface with one SO-DIMM socket per channel. The sockets support the following system memory features.

Table 11: System Memory

Feature	Remark
Socket	2x SO-DIMM DDR4
Memory Type	standard: 1x SO-DIMMs DDR4, max 32 GB per DIMM 2133/2400/2660[1] MHz non-ECC/ECC extended: Up to 4x SO-DIMMs[2] DDR4, max 32 GB per DIMM 2133/2400/2660[1] MHz non-ECC/ECC
Memory Module Size	4 GB, 8 GB, 16 GB, 32 GB
Bandwidth	34.1 Gb/s at 2133 MT/s

Note 1: Memory Speed of 2660 MHz is only supported on 1 DPC (DIMM Per Channel) configurations

Note 2: Second SO-DIMM (bottom side of module) on Channel 2 exceeds the maximum height for COM Express Modules. Special care has to be taken for the Carrier Board design.

2.3.7. Hardware Monitor (HWM)

The Nuvoton NCT7802Y is a hardware monitoring IC, capable of monitor critical system parameters including power supply voltages, fan speeds, and temperatures. The SM-Bus Adress is 5C.

2.3.8. Trusted Platform Module (TPM)

The SLB 9670 is a Trusted Platform Module and is based on advanced hardware security technology. This TPM implementation has achieved CC EAL4+ certification and serves as a basis for other TPM products and firmware upgrades. The Infineon SLB9670 (TPM 2.0) is connected to BOOT SPI0.

2.3.9. SPI BIOS Memory

The Dual 16 MB SPI Flashes is connected to PCH's BOOT SPI0. Failsafe Operation (automatic switchover) can be implemented on request.

2.3.10. Onboard FAN connector

The analog output voltage on this connector is generated via a discrete linear voltage regulator from the PWM signal of the HWM. It is clipped at 12 V (+/- 10 %) across the whole input range of the module to prevent FAN damage at higher voltages.

The maximum supply current to the fan connected to the on-module fan connector is 350 mA if the input voltage is below 13.0 V and is further limited to 150 mA if the input voltage to the module is between 13.0 V and 20.0 V.

Table 12: Onboard FAN connector

Pin	Signal	Description	Type
1	FAN_TACH_IN#	Fan input voltage from COMe connector	Input
2	V_FAN	12 V ±10% (max.) across module input range	PWR
3	GND	Power GND	PWR

2.3.11. General Purpose PCI Express 3.0

Table 13: General Purpose PCI Express 3.0

COMe connector	PCH HSIO Port	PCH I/O Function	Lane Config		Intel RST/Optane
PCIE0	26	PCIE21	x1	x4	YES
PCIE1	27	PCIE22	x1		
PCIE2	28	PCIE23	x1		
PCIE3	29	PCIE24	x1		
PCIE4	18	PCIE13	x1	x4	NO
PCIE5	19	PCIE14	x1		
PCIE6	20	PCIE15	x1		
PCIE7	21	PCIE16	x1		

2.3.12. PCI Express Graphics 3.0 (PEG)

Table 14: PCI Express Graphics 3.0

COMe Lane	1x16 (Default)	1x16 Reversed	2x8	2x8 Reversed	1x8+2x4	1x8+2x4 Reversed
PEG0	0	15	0	7	0	3
PEG1	1	14	1	6	1	2
PEG2	2	13	2	5	2	1
PEG3	3	12	3	4	3	0
PEG4	4	11	4	3	4	3
PEG5	5	10	5	2	5	2
PEG6	6	9	6	1	6	1
PEG7	7	8	7	0	7	0
PEG8	8	7	0	7	0	7
PEG9	9	6	1	6	1	6
PEG10	10	5	2	5	2	5
PEG11	11	4	3	4	3	4
PEG12	12	3	4	3	0	3
PEG13	13	2	5	2	1	2
PEG14	14	1	6	1	2	1
PEG15	15	0	7	0	3	0

2.3.13. Universal Serial Bus (USB)

The device offers up to

- 8x USB 2.0 or
- 4x USB 3.1 with up to 10 Gbit/s.

For every USB 3.1 port, one USB2 and one USB31 lane has to be bonded. Therefore the number of available USB 2.0 ports decreases with every used 3.1 port.

Table 15: Universal Serial Bus (USB)

COMe USB2	COMe USB3	PCH USB2	PCH USB31
USB0	USB_SS0	USB2_1	USB31_1
USB1	USB_SS1	USB2_2	USB31_2
USB2	USB_SS2	USB2_3	USB31_3
USB3	USB_SS3	USB2_4	USB31_4
USB4	-	USB2_5	-
USB5	-	USB2_6	-
USB6	-	USB2_7	-
USB7	-	USB2_8	-

Note: Intel starts counting USB Ports with 1 while COMe Specification starts counting with 0

Table 16: USB Overcurrent

COMe connector	PCH
USB_OC_0_1#	USB2_OC0#
USB_OC_2_3#	USB2_OC1#
USB_OC_4_5#	USB2_OC2#
USB_OC_6_7#	USB2_OC3#

2.3.14. Serial ATA 3.0

Table 17: Serial ATA 3.0

COMe Port	HSIO Port
SATA0	16
SATA1	17
SATA2	22
SATA3	23

2.3.15. Gigabit Ethernet

Intel Jacksonville I219LM Ethernet Connection (PHY only) is connected to PCH HSIO Port 10 (PCIe #5).

Ethernet connectivity is achieved via a single-port integrated physical layer (PHY) supporting Ethernet Media Dependent Interfaces [0-3]. One 10/100/1000 Mbit Ethernet LAN port is available on high-speed I/O port 11.

Table 18: Supported Ethernet Features

Ethernet	10 Base-T/100 Base-TX and 1000 Base-T
Ethernet Controller	Intel® i219LM

Additional features of the Ethernet controller are:

- Intel® vPRO™
- Energy Efficient Ethernet (IEEE 802.3az)
- Intel® SIPP Server Operating System Support
- Jumbo frames (up to 9 kB)
- Reduced power consumption during normal operation
- Integrated Intel® Auto Connect Battery Saver (ACBS)

If the LAN-Cable is disconnected, the ULP (Ultra Low Power) driver featured in Windows 10 **can cause undefined LED behavior. To disable ULP use the "Intel ULPEnable Utility 1.3". For** more information refer to the EMD Customer Section or contact JUMPtec Support.

2.3.16. Graphic Interfaces

Up to four independent Digital Display Interfaces can be used simultaneously and in combination, to implement an independent or cloned display configuration.

- 3x DP 1.2 with Audio
- 1x eDP 1.4 or LVDS
- Optional VGA via a DP 2VGA converter

Table 19: Digital Display Interfaces Overview

CPU Port	COMe Port	
DDI1	DDI1 (DP++) w. Audio	
DDI2	DDI2 (DP++) w. Audio	
DDI3	DDI3 (DP++) w. Audio	VGA (option)
eDP	LVDS	eDP (option)

2.3.16.1. Display Resolution

The following table lists the maximum display resolutions at a set frequency and bit per pixel (bpp) for the supported display interfaces.

Display Interfaces	Maximum Resolution
eDP	4096 x 2304 (60 Hz, 24 bpp)
DP++	4096 x 2304 (60 Hz, 24 bpp)
HDMI 1.4 (native)	4096 x 2160 (24 Hz, 24 bpp)
HDMI 2.0 (via LS-Pcon)	4096 x 2160 (60 Hz, 24 bpp)
VGA	1920 x 1200 (60 Hz, 24 bpp)

At 4K/UHD resolution, a DisplayPort redriver on the carrier is recommended to increase the link margin.

2.3.17. Video Graphics Array (VGA)

Implemented by Chrontel CH7517 DisplayPort to VGA bridge chip.

- Input: 2 DisplayPort Lanes from CPU DDI3.
- Output: VGA Video + VGA DDC

2.3.18. High Definition (HD) Audio

Table 20: HDA Features

COMe Connector	PCH
HDA_RST#	HDA_RST#
HDA_SYNC	HDA_SYNC
HDA_BITCLK	HDA_BCLK
HDA_SDOUT	HDA_SDO

COMe Connector	PCH
HDA_SDIN[0:1]	HDA_SDI[0:1]
HDA_SDIN2	NC

2.3.19. Inter-Integrated Circuit (I2C)-Bus

Two I2C Buses generated by. I2C is used for attaching lower-speed peripheral ICs to processors and microcontrollers in short-distance, intra-board communication.

2.3.20. Power Supply Control Settings

The power supply control settings are set in the BIOS and enable the module to shut down, rest and wake from standby properly.

Table 21: Implemented Power Supply Control Settings

Function	Pin	Definition
Power Button (PWRBTN#)	Pin B12	To start the module using the power button, the PWRBTN# signal must be at least 50 ms (50 ms ≤ t < 4 s, typical 400 ms) at low level (Power Button Event). Pressing the power button for at least four seconds turns off power to the module (Power Button Override).
Power Good (PWR_OK)	Pin B24	PWR_OK is internally pulled up to 3.3 V and must be at the high level to power on the module. This can be driven low to hold the module from powering up as long as needed. The carrier needs to release the signal when ready. Low level prevents the module from entering the S0 state. A falling edge during S0 will cause a direct switch to S5 (Power Failure).
Reset Button (SYS_RESET#)	Pin B49	When the SYS_RESET# pin is detected active (falling edge triggered), it allows the processor to perform a "graceful" reset, by waiting up to 25 ms for the SMBus to go idle before forcing a reset, even though activity is still occurring. Once the reset is asserted, it remains asserted for 5 ms to 6 ms regardless of whether the SYS_RESET# input remains asserted or not.
SM-Bus Alert (SMB_ALERT#)	Pin B15	With an external battery manager present and SMB_ALERT #connected, the module always powers on even if the BIOS switch "After Power Fail" is set to "Stay Off".

2.3.21. General Purpose IOs (GPIOs)

The eight GPIO pins support four inputs pins (A54 for GPI0, A63 for GPI1, A67 for GPI2 and A85 for GPI3) and four output pins (A93 for GPO0, B54 for GPO1, B57 for GPO2 and B63 for GPO3) by default. The four GPI [0-3] pins are pulled high with a pull-up resistor (e.g. 100 K ohms) and the four GPO [0-3] pins are pulled low with a pull-down resistor (e.g. 100 K ohms) on the module.

To change the default GPIO signal-state users are required to make BIOS and/or OS-driver changes, and additional hardware changes by adding external termination resistors on the carrier board to override the weak on-module pull-up resistors with a lower resistance pull-down (e.g. 10 K ohms), or pull-down resistors with a lower resistance pull-up (e.g. 10 K ohms).

2.3.22. Fan Control

Table 22: Fan Signals

COMe Signal	HWM Pin
FAN_PWMOUT	FANCTL2
FAN_TACHIN	FANIN2

2.3.23. UART Serial Ports

Table 23: UART Signals

COMe Signal	EC/kCPLD function
SER0_TX	po_uart_tx[0]
SER0_RX	po_uart_rx[0]
SER1_TX	po_uart_tx[1]
SER1_RX	po_uart_rx[1]

2.3.24. BIOS/Software Features

Table 24: BIOS and Software Features

Feature	Remark
Supported BIOS EFI	AMI Aptio V UEFI
Software	BIOS/EFI Flash utility for EFI Shell, Windows, Linux BIOS/EFI Utility to configure PCIe mapping BIOS/EFI Utility for customers to implement Bootlogo & customize NVRAM (Setup settings)
OS Support	Windows 10 (IOT) Enterprise x64 (incl. Accelerator Driver for Intel Optane Support) Linux x64 (Yocto based) incl. PLD Driver & Live-CD VxWorks 7.x x64

2.3.25. COMe Features

The following table lists supported COMe specification features. For more information, see the COMe specification.

Table 25: COMe Specification Features

Feature	Remark
SPI	Boot from an external SPI
LPC	Supported
UART	2x UART (RX/TX)
LID Signals	Supported
Sleep Signals	Supported
SMBus	Supported
Audio	HD Audio for external HAD codecs

2.3.26. JUMPtec Features

The following table lists specific JUMPtec features.

Table 26: JUMPtec Features

Feature	Remark
External I2C Bus	Fast I2C, MultiMaster capable
M.A.R.S. Support	Supported
Embedded API	KEAPI3
Custom BIOS Settings / Flash Backup	Supported
Watchdog Support	Triple Staged

2.4. Electrical Specification

2.4.1. Power Supply Voltage

The supply voltage is applied through the VCC pins (VCC) of the module connector. The COMe-bCL6 supports a power supply input from 8.5 V to 20 V and operation in both single supply and ATX power supply mode.

Table 27: Power Supply Specifications

Feature	Remark
Supply Voltage Range (VCC)	8.5 V to 20 V for commercial temperature range
Supply Voltage (VCC)	12 V for EXT/E2S variants
Standby Voltage	5 V DC +/- 5 %
RTC	2.5 V to 3.3 V

5 V Standby voltage is not mandatory for operation.
Extended temperature variants are validated for 12 V supply only.

2.4.2. Power Supply Rise Time

The input voltage rise time is 0.1 ms to 20 ms from input voltage ≤10 % to nominal VCC. To comply with the ATX specification there must be a smooth and continuous ramp of each DC input voltage from 10 % to 90 % of the DC input voltage final set point.

2.4.3. Power Supply Voltage Ripple

The maximum power supply voltage ripple is 200 mV peak-to-peak at 0 MHz to 20 MHz.

2.4.4. Power Consumption

Table 28: Single Supply Current Consumption @ 12 V with AVX2 Load

Processor	State	RMS	Peak
E-2176M	Turbo Boost	13.0 A	18.8 A
	Steady State	6.0 A	7.3 A
i5-8400H	Turbo Boost	10.0 A	14.2 A
	Steady State	6.0 A	7.7 A
i7-8850H	Turbo Boost	11.6 A	18.0 A
	Steady State	5.8 A	7.4 A

For Information on detailed power consumption measurements in all states and benchmarks for CPU, graphics and memory performance, see Application Note at EMD Customer Section.

Table 29: Power Supply and Management

Criteria	Description
Suspend Modes	S0 Normal Operation S3 Suspend to RAM S4 Suspend to Disk (OS Hibernate mode) S5 Soft Off S5eco Mode (optional as untested feat.)
Single Supply	Wide range input 8.5-20 V (for commercial temperature range) 12 V only (for EXT/E2S variants)
ATX Mode	12 V VCC + 5 VSB 5 VSB not mandatory for operation
Power Supply Limits	Voltage Ripple maximum 200 mV peak to peak at 0-20 MHz 0.1 to 20 ms rise time from input voltage ≤10 % to nominal VCC 2 A max inrush current peak on 5 VSB Inrush current peak limit. G3/S5 to S0 acc. SFX Design Guide
Power Features	Module shall power on automatically in single supply operation when VCC is connected (with correct BIOS settings)
LID and Sleep	LID and Sleep signal for external Sleep button and LID switch

NOTICE

If any of the supply voltages drops below the allowed operating level longer than the specified hold-up time, all the supply voltages should be shut down and left OFF for a time long enough to allow the internal board voltages to discharge sufficiently.
If the OFF time is not observed, parts of the board or attached peripherals may work incorrectly or even suffer a reduction of MTBF.
The minimum OFF time depends on the implemented PSU model and other electrical factors and needs to be measured individually for each case.

2.4.5. Power Management

Power management options are available within the BIOS setup.

Table 30: Power Management Options

Feature	Remark
ACPI Settings	ACPI 6.0
Miscellaneous Power Management	Supported in BIOS setup menu

Within the BIOS setup If VCC power is removed, 5 V ±5 % can be applied to the V_5V_STBY pins to support the following suspend-states:

- Suspend to RAM (S3)
- Suspend-to-disk / Hibernate (S4)
- Soft-off state (S5)

The Wake-Up event (S0) requires VCC power, as the board is running.

2.4.6. Power Supply Control Settings

The following table provides a description of the COMe-bCL6's power supply control settings.

Table 31: Power Supply Control Settings

Feature	Pin	Remark
Power Button (PWRBTN#)	B12	To start the module using the power button, the PWRBTN# signal must be at least 50 ms (50 ms ≤ t < 4 s, typical 400 ms) at low level (Power Button Event). Pressing the power button for at least four seconds turns off power to the module (Power Button Override).
Power Good (PWR_OK)	B24	PWR_OK is internally pulled up to 3.3 V and must be at the high level to power on the module. This can be driven low to hold the module from powering up as long as needed. The carrier needs to release the signal when ready. Low level prevents the COM3-module from entering the S0 state. A falling edge during S0 will cause a direct switch to S5 (Power Failure).
Reset Button (SYS_RESET#)	B49	When the SYS_RESET# pin is detected active (falling edge triggered), it allows the processor to perform a "graceful" reset, by waiting up to 25 ms for the SMBus to go idle before forcing a reset, even though activity is still occurring. Once the reset is asserted, it remains asserted for 5 ms to 6 ms regardless of whether the SYS_RESET# input remains asserted or not.
SM-Bus Alert (SMB_ALERT#)	B15	With an external battery manager present and SMB_ALERT #connected, the module always powers on even if the BIOS switch "After Power Fail" is set to "Stay Off".

2.4.7. Power Supply Modes

2.4.7.1. ATX Mode

By connecting an ATX power supply with VCC and 5 VSB, PWR_OK is set to low and VCC is off. Pressing the power button sets the ATX PSU setting PWR_OK to high and powers VCC. The PS_ON# signal generated by SUS_S3# (A15) indicates that the system is in Suspend to RAM state. An inverted copy of SUS_S3# on the carrier board may be used to enable non-standby power on a typical ATX supply.

The input voltage must always be higher than 5 V Standby (VCC > 5 VSB) on Computer-on-Modules supporting a wide input voltage range down to 4.75 V.

Table 32: ATX Mode Settings

State	PWRBTN#	PWR_OK	V5_StdBy	PS_ON#	VCC
G3	x	x	0V	x	0V
S5	high	low	5V	high	0V
S5 → S0	PWRBTN Event	low → high	5V	high → low	0 V→ VCC
S0	high	high	5V	low	VCC

(x) – Defines that there is no difference if connected or open.

2.4.7.2. Single Supply Mode

In single supply mode, without 5V standby the module starts automatically when VCC power is connected and Power Good input is open or at high level (internal PU to 3.3 V). PS_ON# is not used in this mode and VCC can be 8.5 V to 20 V.

To power on the module from the S5 state, press the power button or reconnect VCC. Suspend/Standby states are not supported in single supply mode.

Table 33: Single Supply Mode Settings

State	PWRBTN#	PWR_OK	V5_StdBy	VCC
G3	0V/x	0V/x	0V/x	0V/x
G3 → S0	high	open / high	open	connecting VCC
S5	high	open / high	open	VCC
S5 → S0	PWRBTN event	open / high	open	reconnecting VCC

(x) – Defines that there is no difference if connected or open.

All ground pins must be connected to the **carrier board's** ground plane.

Some modules make two or more resets at the first boot in the carrier until everything is initialized. This is usually the case when the customer takes the module out of the box and boots it for the first time. If the power button is then pressed (or pulled via FPGA), this can very probably lead to a malfunction. By default the boards have the option "State After G3", which is set to "S0". The boards boot as soon as they are connected to an ATX power supply. Set this option on the BCL6 under "Chipset" - "PCH-IO Configuration" to "S5" and the board only starts by pressing the Power button.

2.5. Thermal Management

2.5.1. Heatspreader and Cooling Solutions

A heatspreader plate assembly is available from JUMPtec for the COMe-bCL6. The heatspreader plate on top of this assembly is NOT a heat sink. The heatspreader works as a COM Express® standard thermal interface to be use with a heat sink or external cooling devices.

External cooling must be provided to maintain the heatspreader plate at proper operating temperatures. Under worst-case conditions, the cooling mechanism must maintain an ambient air temperature and the heatspreader plate's surface temperature must remain under the maximum temperature range.

You can use many thermal-management solutions with heatspreader plates, including active and passive approaches.

The optimum cooling solution varies, depending on the COM Express® application and environmental conditions. Active or passive cooling solutions provided from JUMPtec for the COMe-bCL6 are usually designed to cover the power and thermal dissipation for a commercial temperature range used in housing with proper airflow.

2.5.2. Operating with JUMPtec Heatspreader Plate (HSP) Assembly

The operating temperature defines two requirements:

- Maximum ambient temperature with ambient being the air surrounding the module
- Maximum measurable temperature on any spot on the heatspreader's surface

The heatspreader is tested for the following temperature specifications.

Table 34: Heatspreader Test Temperature Specifications

Temperature Specification	Validation requirements
Commercial Grade	at 60°C HSP temperature the CPU @ 100% load needs to run at nominal frequency
Extended Temperature (E1)	at 75°C HSP temperature the CPU @ 75% load is allowed to start speedstepping for thermal protection
Industrial Grade by screening (E2S)	at 85°C HSP temperature the CPU @ 50% load is allowed to start throttling for thermal protection

2.5.3. Operating without JUMPtec Heatspreader Plate Assembly

The operating temperature is the maximum measurable temperature on any spot on the module's surface.

2.5.4. On-board Fan Connector

The modules 3-pin fan connector powers, controls and monitors a fan for chassis ventilation.

Fan connector specification:

- Part number (Molex) J3: 53261-0371
- Mates with: 51021-0300
- Crimp terminals: 50079-8100

Table 35: 3-Pin Fan Connector Pin Assignment:

Pin	Signal	Description	Type
1	Fan_Tach_IN#	Input voltage	I
2	V_FAN	Limited to a max. 12 V (±10%) across the whole input range	PWR
3	GND	Power GND	PWR

To connect a standard 3-pin connector fan to the module, use one of the following adaptor cables:

- KAB-HSP 200 mm (PN 96079-0000-00-0)
- KAB-HSP 40 mm (PN 96079-0000-00-2)

If the input voltage is below 13 V, the maximum supply current to the on-module fan connector is 350 mA. The maximum supply current is limited to 150 mA if the input voltage is between 13 V and 20 V.

NOTICE Always check the fan specification according to the limitations of the output current.

Table 36: Electrical Characteristics of the Fan Connector

Fan Power Supply	Input Voltage Range	Input Voltage Range
Module Input Voltage	4.75 V to 13 V	13 V to 20 V
Fan Output Voltage	4.75 V to 13 V	12 V (+/- 10%)
Fan Output Current	350 mA maximum	150 mA

To connect a standard 3-pin connector fan to the module, use one of the following adaptor cables:

- KAB-HSP 200 mm (PN 96079-0000-00-0)
- KAB-HSP 40 mm (PN 96079-0000-00-2)

2.6. Environmental Specification

2.6.1. Temperature

JUMPtec defines the following temperature grades for Computer-on-Modules. For more information on the available temperature grades for the COMe-bCL6, see Chapter 2.1 Module Variants.

Table 37: Temperature Grade Specifications

Temperature Grades	Operating	Storage (Non-operating)	Validated Input Voltage
Extended Temperature (E1)	-25°C to +75°C	-30°C to +85°C	VCC: 12 V
Industrial Grade by Screening (E2S)	-40°C to +85°C (or custom)	-40°C to +85°C	VCC: 12 V

2.6.2. Humidity

Table 38: Humidity Specifications

Humidity
93% at 40°C non-condensing (according to IEC 60068-2-78)

2.7. Standards and Certifications

The COMe-bCL6 complies with the following standards and certifications. All Peripheral interfaces intended for connection to external equipment are ESD/EMI protected.

Table 39: Standards and Certifications

Emission (EMC)	EN55032:2015 Class B Information technology equipment, radio disturbance characteristics- limits and methods of measurement IEC 61000-6-3 :2006 + A1:2010 + AC: 2011 / EN 61000-6-3 :2007 + A1:2011 + AC:2012 EMC generic emissions standard for residential commercial and light industrial environments
Immunity (EMI)	IEC / EN 61000-6-2 : 2005 EMC generic standards immunity for industrial environments Includes the following tests: IEC / EN 61000-4-2 - Electrostatic discharge immunity ESD IEC / EN 61000-4-3 - Radiated field immunity IEC / EN 61000-4-4 - Electrical fast transient/burst (EFT) burst IEC / EN 61000-4-5 - Surge immunity test IEC / EN 61000-4-6 - Immunity to conducted disturbances IEC / EN 61000-4-8 - Power frequency magnetic field Immunity IEC / EN 61000-4-11 - Voltage dips, short interruptions, & voltage variation immunity
Safety	EN 62368-1:2014 Safety for audio/video and information technology equipment
UL	UL 60950-1/CSA 60950-1 Component Recognition Recognized by Underwriters Laboratories Inc. Representative samples of this component have been evaluated by UL and meet applicable UL requirements. UL listings: AZOT2.E147705 AZOT8.E147705
Shock	IEC / EN 60068-2-27 Non-operating shock test – (half-sinusoidal, 11 ms, 15 g)
Vibration	IEC / EN 60068-2-6 Non-operating vibration – (sinusoidal, 10 Hz – 4000 Hz, +/- 0.15 mm, 2 g)
Theoretical MTBF	589864 h @ 40°C (Reliability report article number 38034-0000-27-6) For more details, see Chapter 2.8.
(RoHS II)	2011/65/EU Compliant with the directive on the restriction of the use of certain hazardous substances in electrical and electronic equipment

2.8. MTBF

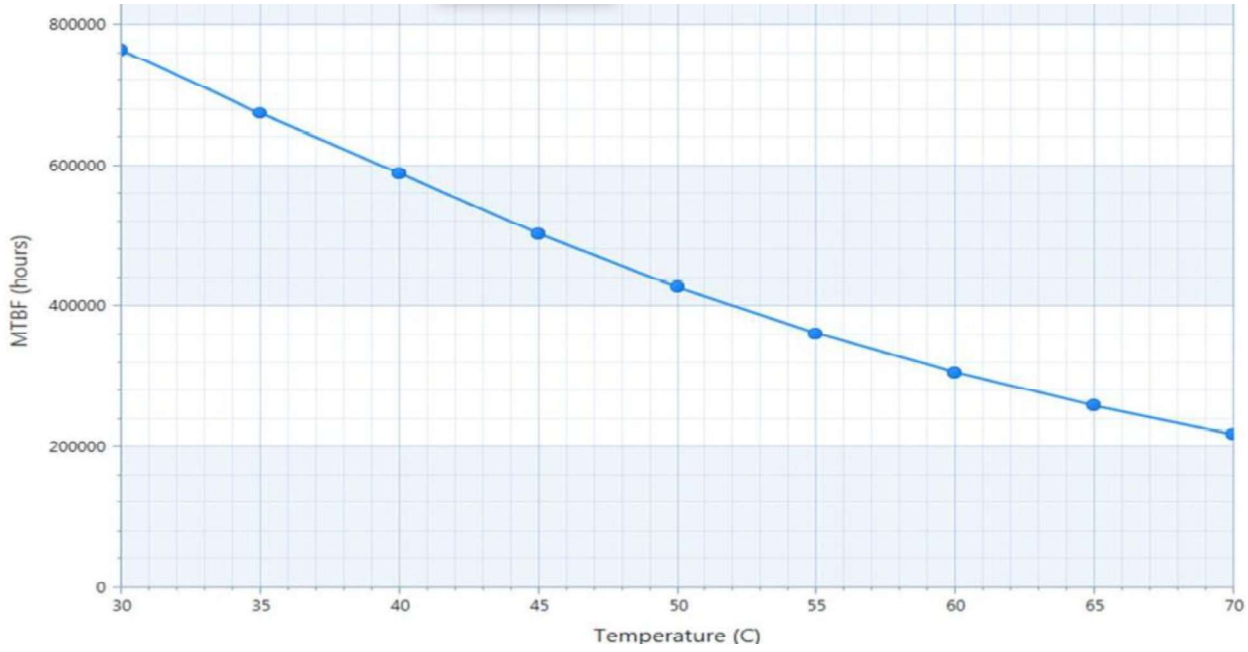
The following MTBF (Mean Time Before Failure) values were calculated using a combination of manufacturer's test data, if the data was available, and the Telcordia (Bellcore) issue 2 calculation for the remaining parts.

The Telcordia calculation used is "Method 1 Case 3" in a ground benign, controlled environment (GB,GC). This particular method takes into account varying temperature and stress data and the system is assumed to have not been burned in.

Figure 2 below shows MTBF de-rating for the E1 temperature range in an office or telecommunications environment. Other environmental stresses (such as extreme altitude, vibration, salt-water exposure) lower MTBF values.

System MTBF (hours) = 589864h @ 40°C (Reliability report article number 38034-0000-27-6)

Figure 4: MTBF Temperature de-Rating



The above estimates assume no fan, but a passive heat sinking arrangement. Estimated RTC battery life (as opposed to battery failures) is not accounted for in the above figure and needs to be considered separately. Battery life depends on both temperature and operating conditions. When the JUMPtec unit has external power, the only battery drain is from leakage paths.

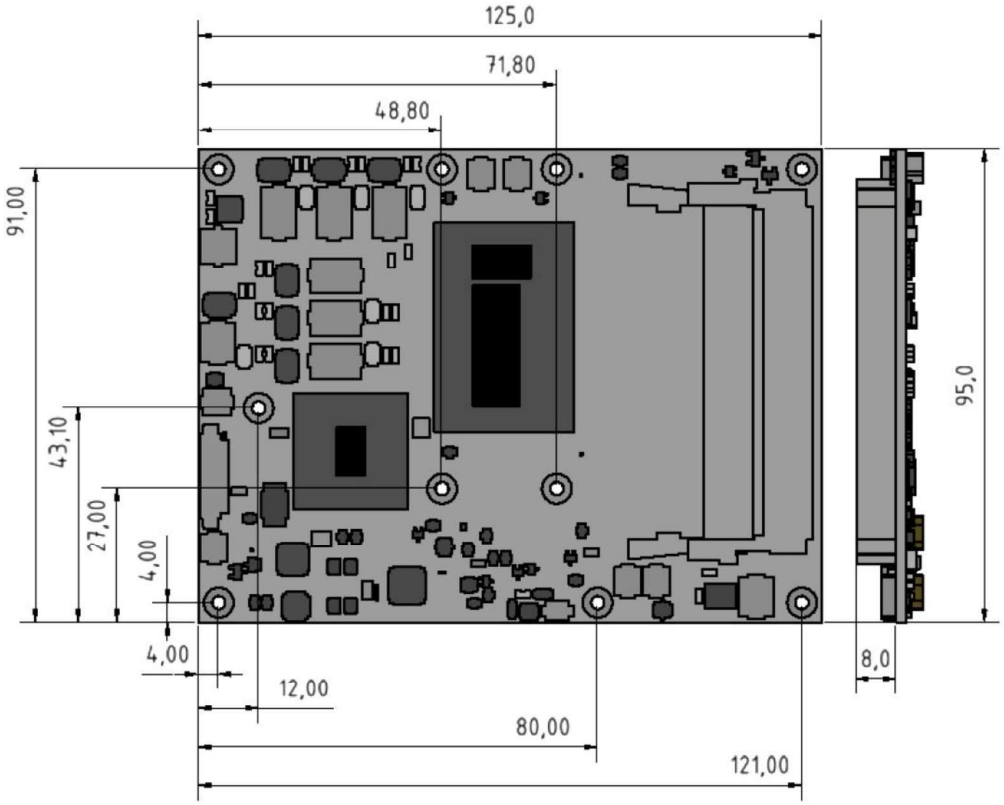
2.9. Mechanical Specification

2.9.1. Dimensions

The dimensions of the module are:

- 95.0 mm x 125.0 mm (3.75 " x 4.92 ")

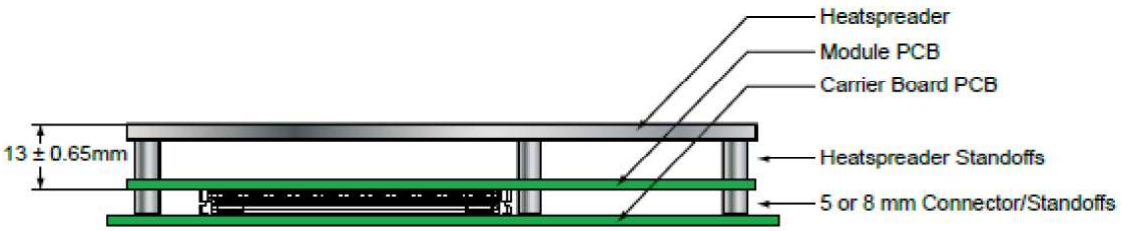
Figure 5: Module Dimensions



2.9.2. Height

The COM Express® specification defines a module height of approximately 13 mm from module PCB bottom to heatspreader top, as shown in the figure below.

Figure 6: Module Height



Cooling solutions provided by JUMPtec for basic sized Computer-on-Modules are 27 mm in height from module bottom to heatsink top. Universal Cooling solutions to be mounted on the heatspreader are 14.3 mm in height for an overall height of 27.3 mm from module bottom to heatsink top.

3/ Features and Interfaces

3.1. LPC

The Low Pin Count (LPC) Interface signals are connected to the LPC Bus bridge located in the CPU or chipset. The LPC low speed interface can be used for peripheral circuits such as an external Super I/O Controller that typically combines legacy-device support into a single IC. The implementation of this subsystem complies with the COM Express® Specification. The COM Express® Design Guide maintained by PICMG provides implementation information or refer to the official PICMG documentation for more information.

The LPC bus does not support DMA (Direct Memory Access). When more than one device is used on LPC, a zero delay clock buffer is required. This leads to limitations for ISA bus and SIO (standard I/O(s) like floppy or LPT interfaces) implementations.

All JUMPtec COM Express® Computer-on-Modules imply BIOS support for the following external baseboard LPC Super I/O controller features for the Winbond/Nuvoton 83627DHG-P.

Table 40: Supported BIOS Features

3.3V 83627DHG-P	AMI EFI APTIO V
PS/2	Not specified
COM1/COM2	Supported
LPT	Supported
HWM	Not supported
Floppy	Not supported
GPIO	Not supported

Features marked as not supported do not exclude OS support (e.g., HWM is accessible via SMB). If any other LPC Super I/O additional BIOS implementations are necessary, contact JUMPtec Support.

3.2. Serial Peripheral Interface (SPI)

The Serial Peripheral Interface Bus (SPI bus) is a synchronous serial data link standard. Devices communicate in master/slave mode, where the master device initiates the data frame. Multiple slave devices are allowed with individual slave select (chip select) lines. SPI is sometimes called a four-wire serial bus, contrasting with three, two and one-wire serial buses.

The SPI interface can only be used with a SPI flash device to boot from the external BIOS on the baseboard.

3.2.1. SPI boot

The COMe-bCL6 supports boot from a 16 MB 3V serial external SPI Flash. Pin A34 (BIOS_DIS0#) and pin B88 (BIOS_DIS1#) configure the SPI Flash as follows:

Table 41: SPI Boot Pin Configuration

Configuration	BIOS_DIS0#	BIOS_DIS1#	Function
1	open	open	Boot on module BIOS
2	GND	open	Not supported
3	open	GND	Boot on baseboard SPI
4	GND	GND	Not supported

BIOS does not support being split between two chips. Booting takes place either from the module SPI or from the baseboard SPI.

The following table provides a list of supported SPI Boot Flash types for the 8-SOIC package.

Table 42: Supported SPI Boot Flash Types for 8-SOIC Package

Size	Manufacturer	Part Number	Device ID
16 MB	Maxim	MX25L12835F	0x20
16 MB	Winbond	W25Q128FV	0x40
16 MB	Micron	N25Q128A	0xBA
16 MB	ISSI	IS25LP128	0x60

3.2.2. Using an External SPI Flash

Initially, boot on the EFI Shell with an USB key containing the binary used to flash the SPI, plugged in on the system.

Depending on which SPI you would like to flash, you will need to use the (BIOS_DIS1) jumper located on the carrier Topanga Canyon Type 6 (J27).

To flash the carrier or module Flash chip:

1. Connect a SPI flash with the correct size (similar to BIOS binary (*.BIN) file size) to the carrier SPI interface.
2. Open pin A34 (BIOS_DIS0#) and pin B88 (BIOS_DIS1#) to boot from the module BIOS.
3. Turn on the system and make sure your USB is connected then start the setup. (See Chapter6.1 Starting the uEFI BIOS).
4. Check that the following entries are set to their default setting:

   Advanced > PCH FW Configuration > Firmware update configuration > ME FW Image Re-Flash > Disabled

   Advanced > PCH FW Configuration > Firmware update configuration > Local FW Update > Enabled

   Then, change the setup option:

   Chipset > PCH-IO Configuration > BIOS Security Configuration > BIOS Lock > Disabled
5. Save and exit setup.
6. Reboot system into EFI shell.
7. Connect pin B88 (BIOS_DIS1#) to ground to enable the external SPI flash.
8. From the EFI shell, enter the name of the partition of your USB Key in this example; Hit FS0: then enter.
9. Type `fpt -SAVEMAC -F BCL6R<xxx>.bin`
10. Wait until the program ends properly and then power cycle the whole system.

The system is now updated.

Depending on the state of the external SPI flash, the program may display up to two warning messages printed in red. Do not stop the process at this point! After a few seconds of timeout, flashing proceeds. For more information, refer to the EMD Customer Section.

3.2.3. External SPI flash on Modules with Intel® ME – in the PRD

If booting from the external (baseboard mounted) SPI flash then exchanging the COM Express® module for another module of the same type will cause the Intel® Management Engine (ME) to fail during the next start. This is due to the design of the ME that bounds itself to every module to which it was previously flashed. In the case of an external SPI flash, this is the module present at flash time.

To avoid this issue, conduct a complete flash of the external SPI flash device after changing the COM Express® module for another module. If disconnecting and reconnecting the same module again, this step is not necessary.

3.2.4. External BIOS ROM Support/SPI

Boot SPI0 is routed to COMe connector. BOM option allows general purpose SPI (GSPI0) to be connected to COMe instead. COMe-bCL6 supports on-module and off-module boot from SPI. For additional safety, a second on-module SPI flash can be populated on the board on customer request.

3.3. M.A.R.S.

The smart battery implementation for JUMPtec Computer-on-Modules called Mobile Application for Rechargeable Systems (M.A.R.S.) is a BIOS extension for an external smart battery manager or charger. M.A.R.S. includes support for a SMBus charger/selector (e.g. Linear Technology LTC1760 Dual Smart Battery System Manager) and provides ACPI compatibility to report battery information to the operating system.

Table 43: Reserved SM-Bus Addresses for Smart Battery Solutions on the Carrier

8-bit Address	7-bit Address	Device
12h	0x09	SMART_CHARGER
14h	0x0A	SMART_SELECTOR
16h	0x0B	SMART_BATTERY

3.4. Fast I2C

Fast I2C supports transfer between components on the same board. The COMe-bCL6 features an on-board I2C controller connected to the LPC Bus.

The I2C controller supports:

- Multimaster transfers
- Clock stretching
- Collision detection
- Interruption on completion of an operation

3.5. UART

The UART implements an interface for serial communications and supports up to two serial RX/TX ports defined in the COM Express® specification on pin A98 (SER0_TX) and pin A99 (SER0_RX) for UART0, and pin A101 (SER1_TX) and pin A102 (SER1_RX) for UART1. The UART controller is fully 16550A compatible.

UART features are:

- On-Chip bit rate (baud rate) generator
- No handshake lines
- Interrupt function to the host
- FIFO buffer for incoming and outgoing data

3.6. Triple Staged Watchdog Timer (WDT)

3.6.1. Basics

A watchdog timer or (computer operating properly (COP) timer) is a computer hardware or software timer. If there is a fault condition in the main program, the watchdog triggers a system reset or other corrective actions. The intention is to bring the system back from the nonresponsive state to normal operation.

Possible fault conditions are a hang, or neglecting to service the watchdog regularly. Such as writing a "service pulse" to it, also referred to as "kicking the dog", "petting the dog", "feeding the watchdog" or "triggering the watchdog".

The COMe-bCL6 offers a watchdog that works with three stages that can be programmed independently and used stage by stage.

Table 44: Triple Stage Watchdog Timer- Time-out Events

0000b	No action	The stage is off and will be skipped.
0001b	Reset	A reset restarts the module and starts a new POST and operating system.
0010b	NMI	A non-maskable interrupt (NMI) is a computer processor interrupt that cannot be ignored by standard interrupt masking techniques in the system. It is used typically to signal attention for non-recoverable hardware errors.
0011b	SMI	A system management interrupt (SMI) makes the processor entering the system management mode (SMM). As such, specific BIOS code handles the interrupt. The current BIOS handler for the watchdog SMI currently does nothing. For special requirements, contact JUMPtec Support.
0100b	SCI	A system control interrupt (SCI) is a OS-visible interrupt to be handled by the OS using AML code.
0101b	Delay -> No action*	Might be necessary when an operating system must be started and the time for the first trigger pulse must be extended. Only available in the first stage.
1000b	WDT Only	This setting triggers the WDT Pin on the baseboard connector (COM Express® pin B27) only.
1001b	Reset + WDT	
1010b	NMI + WDT	
1011b	SMI + WDT	
1100b	SCI + WDT	
1101b	DELAY + WDT -> No action*	

3.6.2. WDT Signal

Watchdog time-out event (pin B27) on COM Express® connector offers a signal that can be asserted when a watchdog timer has not been triggered with a set time. The WDT signal is configurable to any of the three stages. After reset, the signal is automatically deactivated. If deactivation is necessary during runtime, Contact JUMPtec Support for further help.

3.7. Real Time Clock (RTC)

The RTC keeps track of the current time accurately. The RTC's low power consumption means that the RTC can be powered from an alternate source of power enabling the RTC to continue to keep time while the primary source of power is off or unavailable. The COMe-bCL6's RTC battery voltage range is 2.5 V to 3.3 V.

3.8. Rapid Shutdown

The rapid shutdown function is no longer supported.

Please refer to the PCN BCL6V220.

3.8.1. Crowbar implementation details

As a tool for designing the internal crowbars, JUMPtec developed the total capacitance present on each of the internal power rails, and calculates the required discharge resistance in order to achieve the desired voltage decay time constant. The principal design criteria are that each supply rail must decay to 37 % of initial value (equivalent to 1RC) within 250 µs, and to below 1.5 V within 2 ms. Analysis shows that the power rails fall into four general classes. Each class of power rails has a corresponding discharge strategy.

1) Power Input Rails: The main 12 V power input rail incorporates about 300 µF of distributed capacitance. This rail must be discharged by an external crowbar located on the carrier board, which must provide a shunt resistance of approximately 1 Ohm. The peak power dissipation in this crowbar resistance will be relatively high (on the order of 150 W when the crowbar is activated), but will diminish very rapidly as the input capacitors discharge.

2) Low Voltage, High Power Rails: Each of these five "major" internal supply rails has an output voltage in the 1.0 V to 1.5 V range, and each rail has between 1500 µF and 3300 µF of output capacitance. The required discharge resistances for these rails are in the range of 0.1 to 0.2 Ohm, and peak discharge currents are in the range of 8 A to 16 A.

The discharge circuit for each rail is implemented with a "pulse withstanding" thick-film SMT resistor in series with a low-RDSon MOSFET. The resistor peak powers are in the 8 W to 20 W range; depending on PCB layout considerations either a single resistor or multiple smaller resistors may be used to achieve sufficient pulse handling capability.

Because of the relatively high currents in the discharge paths, these crowbar circuits require wide copper traces and careful component placement adjacent to the output components of the corresponding power supplies.

3) Low Voltage, Low Power Rails: These rails have voltages of 1.8 V or less and capacitances under 1000 µF, with peak discharge currents <3A. The discharge circuits for these rails are also implemented with resistor(s) and a low-RDSon MOSFET. In some cases, the peak pulse power dissipation in the resistor(s) is low enough that specialty "pulse withstanding" resistors are not required.

4) Medium Voltage Rails: These 3.3 V and 5 V rails typically have relatively small output capacitances and peak discharge currents <1 A. The discharge circuits for these rails are typically implemented with conventional resistor(s) and a low- RDSon MOSFET.

3.8.2. Shutdown input circuit details

The shutdown input pin to the R E2S module is coupled through a series Schottky diode and a small series resistor to the gates of all crowbar MOSFETs, connected in parallel. All crowbar MOSFETs are N-channel "logic level" parts that have are specified for operation at Vgs = 4.5 V. Three additional components are connected in parallel between the MOSFET gates and ground:

- » A capacitor that provides energy storage to keep the MOSFETs conducting for several mS after the shutdown signal is de-asserted.
- » A high-value resistor that provides a discharge path for the capacitor as well as a pulldown resistance (to insure that the shutdown circuits remain inactive if the shutdown pin is left floating).
- » A 6.2 V Zener diode that protects the MOSFET gates from damage due to input ESD or input overdrive.

In order to insure that the crowbars do not "fight" active switching regulators while the input capacitors are being discharged, the shutdown circuit rapidly crowbars the 5 V rail, with a time constant < 10 µs. The 5 V rail powers most of the remaining switching regulators, and as its voltage falls below about 4 V those regulators enter under-voltage lockout mode and cease to operate. Additionally, by using the UVLO mechanism in the design of the R E2S module, JUMPtec minimizes the risk of inadvertently affecting the standard power sequencing logic for such R E2S modules. Two of the switching regulators do not require the 5 V supply for operation, and in those two cases it will be necessary to clamp the enable inputs to ground when shutdown begins.

4 / System Resources

4.1. Memory Area

The following table specifies the memory address range and COMe-bCL6 memory usage.

Table 45: Designated memory Locations

Address Range (hex)	Size	Project Usage
Address range (hex)	Size	Project usage
00000000-0009FBFF	639 KB	DOS- (Real mode-) memory
0009FC00-0009FFFF	1 KB	Extended BDA
000A0000-000BFFFF	128 KB	Display memory (legacy)
000C0000-000CBFFF	48 KB	VGA BIOS (legacy)
000CC000-000DFFFF	80 KB	Option ROM or XMS (legacy)
000E0000-000EFFFF	64 KB	System BIOS extended space (legacy)
000F0000-000FFFFF	64 KB	System BIOS base segment (legacy)
00100000-76FFFFFF	118 MB	System memory (Low DRAM)
77000000-77FFFFFF	1 MB	SMM region
78000000-7FFFFFFF	8 MB	VGA memory
80000000-FFF00000	2 GB – 1 MB	PCI memory, other extensions (Low MMIO)
TOLUD		
E0000000-EFFFFFFF	256 MB	PCIe Configuration space
F0000000-FEBFFFFF	236 MB	DMI interface (subtractive decoding)
FEC00000-FEC7FFFF	500 KB	IOxAPIC
FEC80000-FECFFFFF	500 KB	Local (CPU) APIC
FED0x000-FED0x3FF	1 KB	HPET (x=0,1,2,3); x is BIOS defined
FED40000-FED47FFF	32 KB	TPM and Trusted Mobile KBC
FED4C000-FED4FFFF	16 KB	PCH internal
FED50000-FED5FFFF	64 KB	Intel ME
FED70000-FED74FFF	20 KB	Internal security device
FEE00000-FEEFFFFF	1 MB	MSI interrupts
FEF00000-FFDFFFFF	15 MB	DMI interface (subtractive decoding)
FFE00000-FFFFFFFF	2 MB	High BIOS / Boot vector
100000000-17FFFFFFF	2 GB	System memory (High DRAM)
180000000-F00000000	58 GB	High MMIO

4.2. I/O Address Map

The I/O port addresses of the COMe-bCL6 are functionally identical to a standard PC/AT. All addresses not mentioned in this table should be available. We recommend that you do not use I/O addresses below 0100h with additional hardware for compatibility reasons, even if the I/O address is available.

Table 46: Designated I/O Port Addresses

I/O Address Range	General Usage	Project Usage
000-01F	DMA-Controller (Master) (ex 8237)	000h-008h DMA-Controller 009h-00Eh reserved 00Fh-018h DMA-Controller 019h-01Eh reserved 01Fh DMA-Controller
020-021, 024-025, 028-029, 02C-02D, 030-031, 034-035, 038-039, 03C-03D	Interrupt-Controller (Master)(ex 8259)	Interrupt-Controller
02E-02F	SuperIO (Winbond)	External SuperIO (Winbond)
040-043, 050-053	Programmable Interrupt Timer (ex 8254)	040h-042h Timer/Counter 043h reserved 040h-042h Timer/Counter 053h reserved
04E-04F	2nd SuperIO (Winbond etc)	None
060, 064	KBD Interface-Controller (ex 8042)	Microcontroller
061, 063, 065, 067	NMI Controller	061h NMI Controller
062, 066	Embedded Microcontroller	Microcontroller
070-073	RTC CMOS / NMI mask + RTC extended CMOS	070h reserved 071h-077h RTC CMOS / NMI mask
080	Debug port	Debug port
081-091	DMA controller, LPC, PCI, or PCIe	DMA controller, LPC, PCI, or PCIe
092	Reset-Generator	Reset-Generator
093-09F	DMA controller	DMA controller
0A0-0A1, 0A4-0A5, 0A8-0A9, 0AC-0AD, 0B0-0B1, 0B4-0B5, 0B8-0B9, 0BC-0BD	Interrupt-Controller (Slave) (ex 8259)	Interrupt-Controller
0B2-0B3	APM control	Power management
0C0-0DF	DMA-Controller (Slave) (ex 8237)	0C0h-0D1h DMA controller 0D2h-0DDh reserved 0DEh-0DFh DMA controller
0F0-0FF	FPU (N/A)	#FERR / Interrupt controller
170-177	HDD-Controller IDE1 Master	SATA controller, PCI, or PCIe
1F0-1F7	HDD-Controller IDE0 Master	SATA controller, PCI, or PCIe

I/O Address Range	General Usage	Project Usage
200-207	Gameport Low	Gameport Low
208-20F	Gameport High	Gameport High
220-22F	Soundblaster®	Not used
279	ISA PnP	Not used
278-27F	Parallel port LPT2	Not used
295-296	Hardware monitor (Winbond default)	Hardware monitor on base board if SuperIO present (optional)
2B0-2BF	EGA	Not used
2D0-2DF	EGA	Not used
2E8-2EF	Serial port COM 4	Serial port COM4 (optional)
2F8-2FF	Serial port COM 2	Serial port COM2
300-301	MIDI	Not used
300-31F	System specific peripherals	Not used
370-377	Floppy disk controller	Optionally used by external (baseboard) SuperIO (370h to 371h)
376-377	HDD-Controller IDE1 Slave	SATA controller, PCI, or PCIe
378-37F	Parallel port LPT 1	LPT1 (if SuperIO present)
3B0-3BB	VGA	VGA (optional)
3BC-3BF	Parallel port LPT3	Not used
3C0-3CF	VGA/EGA	VGA/EGA
3D0-3DF	CGA	VGA (optional)
3E0-3E1	PCMCIA ExCA interface	Not used
3E8-3EF	Serial port COM3	Serial port COM3 (optional)
3F0-3F7	Floppy Disk Controller	Not used
3F6-3F7	HDD controller IDE0 Slave	SATA controller, PCI, or PCIe
3F8-3FF	Serial Port COM1	Serial port COM1
4D0-4D1	Interrupt-Controller (Slave)	Interrupt-Controller (Slave)
A80-A81	JUMPtec CPLD	JUMPtec CPLD control+data port
CF8	PCI configuration address	PCI configuration address
CF9	Reset control	Reset control
CFC-CFF	PCI configuration data	PCI configuration data

Other PCI device I/O addresses are allocated dynamically and not listed here. For more information on how to determine I/O address usage, refer to the OS documentation.

4.3. Legacy Interrupt (IRQ) lines

The following table specifies the Interrupt lines and the device connected to the Interrupt line. It also states which Interrupt lines are available for new devices.

Table 47: List of Interrupt Requests

IRQ	General Usage	Project Usage
0	Timer	Timer
1	Keyboard	Keyboard (SuperIO)
2	Redirected secondary PIC	Redirected secondary PIC
3	COM2	COM2
4	COM1	COM1
5	LPT2/PCI devices	One of COM3+4
6	FDD	One of COM3+4 or not used
7	LPT1	LPT1 or one of COM3+4
8	RTC	RTC
9	SCI / PCI devices	Free for PCI devices
10	PCI devices	Free for PCI devices
11	PCI devices	Free for PCI devices
12	PS/2 mouse	Free for PCI devices
13	FPU	FPU
14	IDE0	Not used
15	IDE1	Not used

4.4. Peripheral Component Interconnect (PCI) Devices

All devices follow the Peripheral Component Interconnect 2.3 (PCI 2.3) and PCI Express Base 1.0a specification. The BIOS and Operating Software (OS) control the memory and I/O resources. For more information, refer to the PCI 2.3 specification.

4.5. I2C Bus

The following table provides details of the devices connected the I2CBus and the I2C address

Table 48: I2C Bus Port Addresses

I2C Address	Used For	Available	Comment
58h		No	Internally reserved
A0h	JIDA-EEPROM	No	Module EEPROM
AEh	FRU-EEPROM	No	Recommended for Baseboard EEPROM

4.6. System Management (SM) Bus

The 8-bit SMBus address uses the LSB (Bit 0) for the direction of the device.

- Bit0 = 0 defines the write address
- Bit0 = 1 defines the read address

The 8-bit address listed below shows the write address for all devices. The7-bit SMBus address shows the device address without bit0.

Table 49: Designated I/O Port Addresses

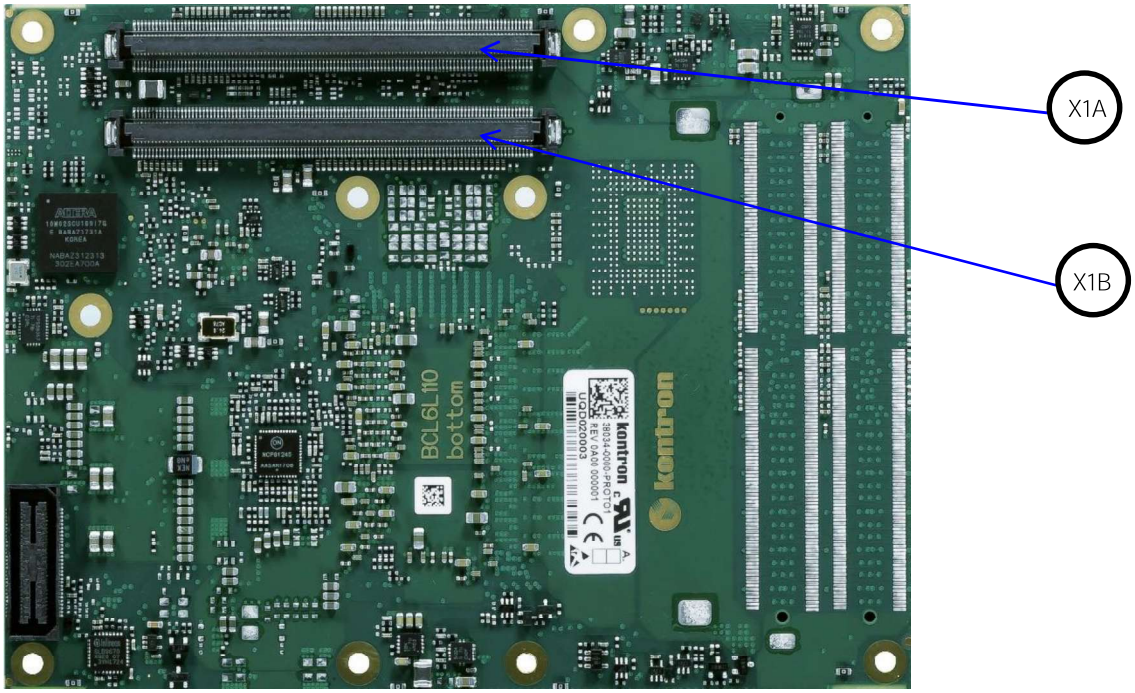
8-bit Address	7-bit Address	Device	Comment	SMBus
5Ch	2Eh	HWM NCT7802Y	Do not use under any circumstances	SMB
A0h	50h	SPD DDR Channel 1 (SO-DIMM)		SMB
A4h	52h	SPD DDR Channel 2 (SO-DIMM)		SMB
30h	18h	SO-DIMM Thermal Sensor	If available on the used memory-module	SMB
34h	1Ah	SO-DIMM Thermal Sensor channel 2	If available on the used memory-module	SMB

5/ Interface Connectors X1A and X1B

The COMe-bCL6 is a COM Express® basic module containing two 220-pin connectors; each with two rows called row A & B on primary connector and row C & D on secondary connector.

The following figure is a view of the bottom of the module showing the position of interface connectors X1A and X1B.

Figure 7: X1A and X1B COMe Interface Connectors



5.1. X1A and X1B Signals

For a description of the terms used in the X1A and X1B pin assignment tables, see the General Signals Description table below or Appendix A, List of Acronyms. If a more detailed pin assignment description is required, refer to the PICMG specification COMe Rev 3.0 Type 6 standard.

The information provided under type, module terminations and comments is complimentary to the COM.0 Rev 3.0 Type 6 standard. For more information, contact JUMPtec Support.

Table 50: General Signal Description

Type	Description	Type	Description
NC	Not Connected (on this product)	O-1,8	1.8 V Output
I/O-3,3	Bi-directional 3.3 V I/O-Signal	O-3,3	3.3 V Output
I/O-5T	Bi-dir. 3.3 V I/O (5 V Tolerance)	O-5	5 V Output
I/O-5	Bi-directional 5V I/O-Signal	DP-I/O	Differential Pair Input/Output
I-3,3	3.3 V Input	DP-I	Differential Pair Input

Type	Description	Type	Description
I/OD	Bi-directional Input/Output Open Drain	DP-O	Differential Pair Output
I-5T	3.3 V Input (5 V Tolerance)	PU	Pull-Up Resistor
OA	Output Analog	PWR	Power Connection
OD	Output Open Drain	+ and -	Differential Pair Differentiator

NOTICE

To protect external power lines of peripheral devices, make sure that: the wires have the right diameter to withstand the maximum available current.

The enclosure of the peripheral device fulfills the fire-protection requirements of IEC/EN60950.

5.2. X1A and X1B Pin Assignment

For more information regarding the pinout of connector X1A (Row A and Row B) and connector X1B (Row C and Row D), see the tables listed below:

- Table 51: Connector X1A Row A Pin Assignment (A1- A110): Connector X1A Row A1 - A110
- Table 52: Connector X1A Row B Pin Assignment (B1-B110): Connector X1A Row B1 - B110
- Table 53: Connector X1B Row C Pin Assignment (C1-C110): Connector X1B Row C1 - C110
- Table 54: Connector X1B Row D Pin Assignment (D1-D110): Connector X1B Row D1 - D110

5.2.1. Connector X1A Row A1 – A110

The following section describes the signals found on COM Express™ Type 6 connectors used for JUMPtec modules. The pinout of the modules complies with COM Express Type 6 Rev. 3.0. The table below describes the terminology used in this section. The PU/PD column indicates if a COM Express™ module pull-up or pull-down resistor has been used. If the field entry area in this column for the signal is empty, then no pull-up or pull-down resistor has been implemented by JUMPtec.

The "#" symbol at the end of the signal name indicates that the active or asserted state occurs when the signal is at a low voltage level. When "#" is not present, the signal is asserted when at a high voltage level.

NOTICE

The Signal Description tables list all internal pull-ups or pull-downs implemented by the chip vendors.

Table 51: Connector X1A Row A Pin Assignment (A1- A110)

Pin	Signal	Description	Type	Termination	Comment
A1	GND	Power Ground	PWR GND	---	---
A2	GBE0_MDI3-	Ethernet Media Dependent Interface 3 -	DP-I/O	---	---
A3	GBE0_MDI3+	Ethernet Media Dependent Interface 3 +	DP-I/O	---	---
A4	GBE0_LINK100#	Ethernet Speed LED	OD	---	---

Pin	Signal	Description	Type	Termination	Comment
A5	GBE0_LINK1000#	Ethernet Speed LED	OD	---	---
A6	GBE0_MDI2-	Ethernet Media Dependent Interface 2 -	DP-I/O	---	---
A7	GBE0_MDI2+	Ethernet Media Dependent Interface 2 +	DP-I/O	---	---
A8	GBE0_LINK#	LAN Link LED	OD	---	---
A9	GBE0_MDI1-	Ethernet Media Dependent Interface 1 -	DP-I/O	---	---
A10	GBE0_MDI1+	Ethernet Media Dependent Interface 1 +	DP-I/O	---	---
A11	GND	Power Ground	PWR GND	---	---
A12	GBE0_MDI0-	Ethernet Media Dependent Interface 0 -	DP-I/O	---	---
A13	GBE0_MDI0+	Ethernet Media Dependent Interface 0 +	DP-I/O	---	---
A14	GBE0_CTREF	Center Tab Reference Voltage	O	---	100 nF capacitor to GND
A15	SUS_S3#	Suspend To RAM (or deeper) Indicator	O-3.3	PD 100k	---
A16	SATA0_TX+	SATA Transmit Pair 0 +	DP-O	---	---
A17	SATA0_TX-	SATA Transmit Pair 0 -	DP-O	---	---
A18	SUS_S4#	Suspend To Disk (or deeper) Indicator	O-3.3	PD 100k	---
A19	SATA0_RX+	SATA Receive Pair 0 +	DP-I	---	---
A20	SATA0_RX-	SATA Receive Pair 0 -	DP-I	---	---
A21	GND	Power Ground	PWR GND	---	---
A22	SATA2_TX+	SATA Transmit Pair 2 +	DP-O	---	---
A23	SATA2_TX-	SATA Transmit Pair 2 -	DP-O	---	---
A24	SUS_S5#	Soft Off Indicator	O-3.3	---	---
A25	SATA2_RX+	SATA Receive Pair 2 +	DP-I	---	---
A26	SATA2_RX-	SATA Receive Pair 2 -	DP-I	---	---
A27	BATLOW#	Battery Low	I-3.3	PU 10k 3.3V (S5)	assertion will prevent wake from S3-S5 state
A28	(S)ATA_ACT#	Serial ATA activity LED	OD-3.3	PU 10k 3.3V (S0)	can sink 15mA
A29	HDA_SYNC	HD Audio Sync	O-3.3	PD 100k	---
A30	HDA_RST#	HD Audio Reset	O-3.3	PD 100k	---
A31	GND	Power Ground	PWR GND	---	---
A32	HDA_CLK	HD Audio Bit Clock Output	O-3.3	PD 20k in PCH	---
A33	HDA_SDOUT	HD Audio Serial Data Out	O-3.3	PD 20k in PCH	---
A34	BIOS_DIS0#/ESPI_SAFS	BIOS Selection Strap 0	I-3.3	PU 10k 3.3V (S5)	---

Pin	Signal	Description	Type	Termination	Comment
A35	THRMTRIP#	Thermal Trip	O-3.3	PU 10k 3.3V (S0)	Thermal Trip Event, transition to S5 indicator
A36	USB6-	USB 2.0 Data Pair Port 6 –	DP-I/O	PD 14.25k to 24.8k in PCH	---
A37	USB6+	USB 2.0 Data Pair Port 6 +	DP-I/O	PD 14.25k to 24.8k in PCH	---
A38	USB_6_7_OC#	USB Overcurrent Indicator Port 6/7	I-3.3	PU 10k 3.3V (S5)	---
A39	USB4-	USB 2.0 Data Pair Port 4 -	DP-I/O	PD 14.25k to 24.8k in PCH	---
A40	USB4+	USB 2.0 Data Pair Port 4 +	DP-I/O	PD 14.25k to 24.8k in PCH	---
A41	GND	Power Ground	PWR GND	---	---
A42	USB2-	USB 2.0 Data Pair Port 2 –	DP-I/O	PD 14.25k to 24.8k in PCH	---
A43	USB2+	USB 2.0 Data Pair Port 2 +	DP-I/O	PD 14.25k to 24.8k in PCH	---
A44	USB_2_3_OC#	USB Overcurrent Indicator Port 2/3	I-3.3	PU 10k 3.3V (S5)	---
A45	USB0–	USB 2.0 Data Pair Port 0 –	DP-I/O	PD 14.25k to 24.8k in PCH	---
A46	USB0+	USB 2.0 Data Pair Port 0 +	DP-I/O	PD 14.25k to 24.8k in PCH	---
A47	VCC_RTC	Real-Time Clock Circuit Power Input	PWR 3V	---	voltage range 2.5 to 3.3 V
A48	RSVD	Reserved for future use	nc	---	---
A49	GBE0_SDP	Gigabit Ethernet Controller 0 Software-Definable Pin	I/O-3.3	---	---
A50	LPC_SERIRQ/ESPI _CS1#	Serial Interrupt Request/eSPI Master Chip Select 1	I/OD-3.3/O-1,8	PU 8k2 3.3V (S0)	---
A51	GND	Power Ground	PWR GND	---	---
A52	PCIE_TX5+	PCI Express Lane 5 Transmit +	DP-O	---	---
A53	PCIE_TX5-	PCI Express Lane 5 Transmit -	DP-O	---	---
A54	GPI0	General Purpose Input 0	I-3.3	PU 100k 3.3V (S0)	---
A55	PCIE_TX4+	PCI Express Lane 4 Transmit +	DP-O	---	---
A56	PCIE_TX4-	PCI Express Lane 4 Transmit -	DP-O	---	---
A57	GND	Power Ground	PWR GND	---	---
A58	PCIE_TX3+	PCI Express Lane 3 Transmit +	DP-O	---	---

Pin	Signal	Description	Type	Termination	Comment
A59	PCIE_TX3-	PCI Express Lane 3 Transmit -	DP-O	---	---
A60	GND	Power Ground	PWR GND	---	---
A61	PCIE_TX2+	PCI Express Lane 2 Transmit +	DP-O	---	---
A62	PCIE_TX2-	PCI Express Lane 2 Transmit -	DP-O	---	---
A63	GPI1	General Purpose Input 1	I-3.3	PU 100k 3.3V (S0)	---
A64	PCIE_TX1+	PCI Express Lane 1 Transmit +	DP-O	---	---
A65	PCIE_TX1-	PCI Express Lane 1 Transmit -	DP-O	---	---
A66	GND	Power Ground	PWR GND	---	---
A67	GPI2	General Purpose Input 2	I-3.3	PU 100k 3.3V (S0)	---
A68	PCIE_TX0+	PCI Express Lane 0 Transmit +	DP-O	---	---
A69	PCIE_TX0-	PCI Express Lane 0 Transmit -	DP-O	---	---
A70	GND	Power Ground	PWR GND	---	---
A71	LVDS_A0+	LVDS Channel A DAT0+/EDP Lane 2 Transmit +	DP-O	---	---
A72	LVDS_A0-	LVDS Channel A DAT0-/EDP Lane 2 Transmit -	DP-O	---	---
A73	LVDS_A1+	LVDS Channel A DAT1+/EDP Lane 1 Transmit +	DP-O	---	---
A74	LVDS_A1-	LVDS Channel A DAT1-/EDP Lane 1 Transmit -	DP-O	---	---
A75	LVDS_A2+	LVDS Channel A DAT2+/EDP Lane 0 Transmit +	DP-O	---	---
A76	LVDS_A2-	LVDS Channel A DAT2-/EDP Lane 0 Transmit -	DP-O	---	---
A77	LVDS_VDD_EN	LVDS/EDP Panel Power Control	O-3.3	PD 100k	---
A78	LVDS_A3+	LVDS Channel A DAT3+	DP-O	---	---
A79	LVDS_A3-	LVDS Channel A DAT3-	DP-O	---	---
A80	GND	Power Ground	PWR GND	---	---
A81	LVDS_A_CK+	LVDS Channel A Clock+/EDP Lane 3 Transmit +	DP-O	---	Clock: 20-80MHz
A82	LVDS_A_CK-	LVDS Channel A Clock-/EDP Lane 3 Transmit -	DP-O	---	Clock: 20-80MHz
A83	LVDS_I2C_CK	LVDS I2C Clock (DDC)/EDP AUX +	I/O-3.3	PU 2k2 3.3V (S0)	---
A84	LVDS_I2C_DAT	LVDS I2C Data (DDC)/EDP AUX -	I/O-3.3	PU 2k2 3.3V (S0)	---
A85	GPI3	General Purpose Input 3	I-3.3	PU 100k 3.3V (S0)	---
A86	RSVD	Reserved for future use	nc	---	---
A87	eDP_HPD	EDP Hot Plug Detect	I-3.3	PD 400k LVDS/100k EDP	---
A88	PCIE_CLK_REF+	Reference PCI Express Clock +	DP-O	---	100MHz
A89	PCIE_CLK_REF-	Reference PCI Express Clock -	DP-O	---	100MHz

Pin	Signal	Description	Type	Termination	Comment
A90	GND	Power Ground	PWR GND	---	---
A91	SPI_POWER	3.3V Power Output Pin for external SPI flash	O-3.3	---	100mA (max.)
A92	SPI_MISO	SPI Master IN Slave OUT	I-3.3	PU 20k +/- 30% in PCH (S5)	All SPI signals are tri-stated until reset is deasserted
A93	GP00	General Purpose Output 0	O-3.3	PD 100k	---
A94	SPI_CLK	SPI Clock	O-3.3	PU 20k +/- 30% in PCH (S5)	All SPI signals are tri-stated with 20k ohm CPU internal weak pull-up until reset is deasserted
A95	SPI_MOSI	SPI Master Out Slave In	O-3.3	PU 20k +/- 30% in PCH (S5)	All SPI signals are tri-stated with 20k ohm CPU internal weak pull-up until reset is deasserted
A96	TPM_PP	TPM Physical Presence	I-3.3	PD 10k	TPM does not use this functionality
A97	TYPE10#	Indicates TYPE10# to carrier board	nc	---	---
A98	SER0_TX	Serial Port 0 TXD	O-3.3	---	20V protection circuit implemented on module, PD on carrier board needed for proper operation
A99	SER0_RX	Serial Port 0 RXD	I-5T	PU 10k 3.3V (S0)	20V protection circuit implemented on module
A100	GND	Power Ground	PWR GND	---	---
A101	SER1_TX	Serial Port 1 TXD	O-3.3	---	20V protection circuit implemented on module, PD on carrier board needed for proper operation
A102	SER1_RX	Serial Port 1 RXD	I-5T	PU 10k 3.3V (S0)	20V protection circuit implemented on module

Pin	Signal	Description	Type	Termination	Comment
A103	LID#	LID Switch Input	I-3.3	PU 47k 3.3V (S5)	20V protection circuit implemented on module
A104	VCC_12V	Main Input Voltage (4.75-20V)	PWR 4.75-20V	---	---
A105	VCC_12V	Main Input Voltage (4.75-20V)	PWR 4.75-20V	---	---
A106	VCC_12V	Main Input Voltage (4.75-20V)	PWR 4.75-20V	---	---
A107	VCC_12V	Main Input Voltage (4.75-20V)	PWR 4.75-20V	---	---
A108	VCC_12V	Main Input Voltage (4.75-20V)	PWR 4.75-20V	---	---
A109	VCC_12V	Main Input Voltage (4.75-20V)	PWR 4.75-20V	---	---
A110	GND	Power Ground	PWR GND	---	---

+ and - Differential pair differentiator

5.2.2. Connector X1A Row B 1 - B 110

Table 52: Connector X1A Row B Pin Assignment (B1-B110)

Pin	Signal	Description	Type	Termination	Comment
B1	GND	Power Ground	PWR GND	---	---
B2	GBE0_ACT#	Ethernet Activity LED	OD	---	---
B3	LPC_FRAME#/ ESPI_CS0	LPC Frame Indicator/eSPI Master Chip Select 0	O-3.3/eSPI O- 1.8	---	---
B4	LPC_AD0/ ESPI_IO_0	LPC Multiplexed Command, Address & Data 0/eSPI Master Data I/O 0	I/O-3.3/eSPI I/O- 1.8	PU 20k 3.3V (S0)	---
B5	LPC_AD1/ ESPI_IO_1	LPC Multiplexed Command, Address & Data 1/eSPI Master Data I/O 1	I/O-3.3/eSPI I/O- 1.8	PU 20k 3.3V (S0)	---
B6	LPC_AD2/ ESPI_IO_2	LPC Multiplexed Command, Address & Data 2/eSPI Master Data I/O 2	I/O-3.3/eSPI I/O- 1.8	PU 20k 3.3V (S0)	---
B7	LPC_AD3/ ESPI_IO_3	LPC Multiplexed Command, Address & Data 3/eSPI Master Data I/O 3	I/O-3.3/eSPI I/O- 1.8	PU 20k 3.3V (S0)	---
B8	LPC_DRQ0#/ ESPI_ALERT0#	LPC Serial DMA/Master Request 0 / eSPI Alert 0	I-3.3/eSPI I-1.8	PU 10k 3.3V (S0)	---
B9	LPC_DRQ1#/ ESPI_ALERT1#	LPC Serial DMA/Master Request 1 / eSPI Alert 1	I-3.3/eSPI I-1.8	PU 10k 3.3V (S0)	---
B10	LPC_CLK/ ESPI_CK	24MHz LPC clock	O-3.3/eSPI O- 1.8		
B11	GND	Power Ground	PWR GND	---	---

Pin	Signal	Description	Type	Termination	Comment
B12	PWRBTN#	Power Button	I-3.3	PU 3k32 3.3V (S5)	
B13	SMB_CLK	SMBUS Clock	O-3.3	PU 3k9 3.3V (S5)	---
B14	SMB_DAT	SMBUS Data	I/O-3.3	PU 3k9 3.3V (S5)	---
B15	SMB_ALERT#	SMBUS Alert	I/O-3.3	PU 2k26 3.3V (S5)	---
B16	SATA1_TX+	SATA 1 Transmit Pair +	DP-O	---	---
B17	SATA1_TX-	SATA 1 Transmit Pair -	DP-O	---	---
B18	SUS_STAT#/ ESPI_RESET#	Suspend Status/eSPI Reset	O-3.3/O-1.8	---	---
B19	SATA1_RX+	SATA 1 Receive Pair +	DP-I	---	---
B20	SATA1_RX-	SATA 1 Receive Pair -	DP-I	---	---
B21	GND	Power Ground	PWR GND	---	---
B22	SATA3_TX+	SATA 3 Transmit Pair +	nc	---	---
B23	SATA3_TX-	SATA 3 Transmit Pair -	nc	---	---
B24	PWR_OK	Power OK	I-5T	PU 51k 3.3V (S5)	20V protection circuit implemented on module
B25	SATA3_RX+	SATA 3 Receive Pair +	nc	---	---
B26	SATA3_RX-	SATA 3 Receive Pair -	nc	---	---
B27	WDT	Watch Dog Time-Out event	O-3.3	PD 10K	---
B28	HDA_SDIN2	Not Connected	nc	---	not supported
B29	HDA_SDIN1	Audio Codec Serial Data in 1	I-3.3	PD 20k in PCH	---
B30	HDA_SDIN0	Audio Codec Serial Data in 0	I-3.3	PD 20k in PCH	---
B31	GND	Power Ground	PWR GND	---	---
B32	SPKR	Speaker	O-3.3	PD 20k +/- 30% in PCH	PD is enabled until reset is deasserted
B33	I2C_CK	I2C Clock	O-3.3	PU 2k21 3.3V (S5)	---
B34	I2C_DAT	I2C Data	I/O-3.3	PU 2k21 3.3V (S5)	---
B35	THRM#	Over Temperature Input	I-3.3	PU 10k 3.3V (S0)	no function implemented
B36	USB7-	USB 2.0 Data Pair Port 7 –	DP-I/O	PD 14.25k to 24.8k in PCH	---
B37	USB7+	USB 2.0 Data Pair Port 7 +	DP-I/O	PD 14.25k to 24.8k in PCH	---

Pin	Signal	Description	Type	Termination	Comment
B38	USB_4_5_OC#	USB Overcurrent Indicator Port 4/5	I-3.3	PU 10k 3.3V (S5)	---
B39	USB5-	USB 2.0 Data Pair Port 5 –	DP-I/O	PD 14.25k to 24.8k in PCH	---
B40	USB5+	USB 2.0 Data Pair Port 5 +	DP-I/O	PD 14.25k to 24.8k in PCH	---
B41	GND	Power Ground	PWR GND	---	---
B42	USB3-	USB 2.0 Data Pair Port 3 –	DP-I/O	PD 14.25k to 24.8k in PCH	---
B43	USB3+	USB 2.0 Data Pair Port 3 +	DP-I/O	PD 14.25k to 24.8k in PCH	---
B44	USB_0_1_OC#	USB Overcurrent Indicator Port 0/1	I-3.3	PU 10k 3.3V (S5)	---
B45	USB1-	USB 2.0 Data Pair Port 1 –	DP-I/O	PD 14.25k to 24.8k in PCH	---
B46	USB1+	USB 2.0 Data Pair Port 1 +	DP-I/O	PD 14.25k to 24.8k in PCH	---
B47	ESPI_EN#	[Enable/Disable] ESPI- Mode/LPC-Mode	I-3.3	PU 10k 1.8V (S5)	---
B48	USB_HOST_PRSNT	USB Host Detection	I-3.3	---	---
B49	SYS_RESET#	Reset Button Input	I-3.3	PU 3k32 3.3V (S5)	---
B50	CB_RESET#	Carrier Board Reset	O-3.3	PD 10k	---
B51	GND	Power Ground	PWR GND	---	---
B52	PCIE_RX5+	PCI Express Lane 5 Receive +	DP-I	---	---
B53	PCIE_RX5-	PCI Express Lane 5 Receive -	DP-I	---	---
B54	GPO1	General Purpose Output 1	O-3.3	PD 100k	---
B55	PCIE_RX4+	PCI Express Lane 4 Receive +	DP-I	---	---
B56	PCIE_RX4-	PCI Express Lane 4 Receive -	DP-I	---	---
B57	GPO2	General Purpose Output 2	O-3.3	PD 100k	---
B58	PCIE_RX3+	PCI Express Lane 3 Receive +	DP-I	---	---
B59	PCIE_RX3-	PCI Express Lane 3 Receive -	DP-I	---	---
B60	GND	Power Ground	PWR GND	---	---
B61	PCIE_RX2+	PCI Express Lane 2 Receive +	DP-I	---	---
B62	PCIE_RX2-	PCI Express Lane 2 Receive -	DP-I	---	---
B63	GPO3	General Purpose Output 3	O-3.3	PD 100k	---
B64	PCIE_RX1+	PCI Express Lane 1 Receive +	DP-I	---	---
B65	PCIE_RX1-	PCI Express Lane 1 Receive -	DP-I	---	---
B66	WAKE0#	PCI Express Wake Event	I-3.3	PU 10k 3.3V (S5)	---

Pin	Signal	Description	Type	Termination	Comment
B67	WAKE1#	General Purpose Wake Event	I-3.3	PU 10k 3.3V (S5)	---
B68	PCIE_RX0+	PCI Express Lane 0 Receive +	DP-I	---	---
B69	PCIE_RX0-	PCI Express Lane 0 Receive -	DP-I	---	---
B70	GND	Power Ground	PWR GND	---	---
B71	LVDS_B0+	LVDS Channel B DAT0+	DP-O	---	---
B72	LVDS_B0-	LVDS Channel B DAT0-	DP-O	---	---
B73	LVDS_B1+	LVDS Channel B DAT1+	DP-O	---	---
B74	LVDS_B1-	LVDS Channel B DAT1-	DP-O	---	---
B75	LVDS_B2+	LVDS Channel B DAT2+	DP-O	---	---
B76	LVDS_B2-	LVDS Channel B DAT2-	DP-O	---	---
B77	LVDS_B3+	LVDS Channel B DAT3+	DP-O	---	---
B78	LVDS_B3-	LVDS Channel B DAT3-	DP-O	---	---
B79	LVDS_BKLT_EN	LVDS/EDP Panel Backlight On	O-3.3	PD 100k	---
B80	GND	Power Ground	PWR GND	---	---
B81	LVDS_B_CK+	LVDS Channel B Clock+	DP-O	---	20-80MHz
B82	LVDS_B_CK-	LVDS Channel B Clock-	DP-O	---	20-80MHz
B83	LVDS_BKLT_CTRL	LVDS/EDP Backlight Brightness Control	O-3.3	---	---
B84	VCC_5V_SBY	5V Standby	PWR 5V (S5)	---	optional (not neccessary in single supply mode)
B85	VCC_5V_SBY	5V Standby	PWR 5V (S5)	---	optional (not neccessary in single supply mode)
B86	VCC_5V_SBY	5V Standby	PWR 5V (S5)	---	optional (not neccessary in single supply mode)
B87	VCC_5V_SBY	5V Standby	PWR 5V (S5)	---	optional (not neccessary in single supply mode)
B88	BIOS_DIS1#	BIOS Selection Strap 1	I-3.3	PU 10k 3.3V (S0)	PU might be powered during suspend
B89	VGA_RED	Analog Video RGB-RED	nc	---	---
B90	GND	Power Ground	PWR GND	---	---
B91	VGA_GREEN	Analog Video RGB-GREEN	nc	---	---
B92	VGA_BLUE	Analog Video RGB-BLUE	nc	---	---
B93	VGA_HSYNC	Analog Video H-Sync	nc	---	---
B94	VGA_VSYNC	Analog Video V-Sync	nc	---	---
B95	VGA_I2C_CLK	Display Data Channel Clock	nc	---	---
B96	VGA_I2C_DATA	Display Data Channel Data	nc	---	---

Pin	Signal	Description	Type	Termination	Comment
B97	SPI_CS#	SPI Chip Select	O-3.3	---	---
B98	RSVD	Reserved for future use	nc	---	---
B99	RSVD	Reserved for future use	nc	---	---
B100	GND	Power Ground	PWR GND	---	---
B101	FAN_PWMOUT	Fan PWM Output	O-3.3	---	20V protection circuit implemented on module, PD on carrier board needed for proper operation
B102	FAN_TACHIN	Fan Tach Input	I-3.3	PU 47k 3.3V (S0)	20V protection circuit implemented on module
B103	SLEEP#	Sleep Button Input	I-3.3	PU 47k 3.3V (S5)	20V protection circuit implemented on module
B104	VCC_12V	Main Input Voltage (4.75-20V)	PWR 4.75-20V	---	---
B105	VCC_12V	Main Input Voltage (4.75-20V)	PWR 4.75-20V	---	---
B106	VCC_12V	Main Input Voltage (4.75-20V)	PWR 4.75-20V	---	---
B107	VCC_12V	Main Input Voltage (4.75-20V)	PWR 4.75-20V	---	---
B108	VCC_12V	Main Input Voltage (4.75-20V)	PWR 4.75-20V	---	---
B109	VCC_12V	Main Input Voltage (4.75-20V)	PWR 4.75-20V	---	---
B110	GND	Power Ground	PWR GND	---	---

+ and -Differential pair differentiator

5.2.3. Connector X1B Row C 1 - C 110

Table 53: Connector X1B Row C Pin Assignment (C1-C110)

Pin	Signal	Description	Type	Termination		Comment
C1	GND	Power Ground	PWR GND	---		---
C2	GND	Power Ground	PWR GND	---		---
C3	USB_SSRX0-	USB Super Speed Receive 0 -	DP-I	---		---
C4	USB_SSRX0+	USB Super Speed Receive 0 +	DP-I	---		---

Pin	Signal	Description	Type	Termination		Comment
C5	GND	Power Ground	PWR GND	---		---
C6	USB_SSRX1-	USB Super Speed Receive 1 -	DP-I	---		---
C7	USB_SSRX1+	USB Super Speed Receive 1 +	DP-I	---		---
C8	GND	Power Ground	PWR GND	---		---
C9	USB_SSRX2-	USB Super Speed Receive 2 -	DP-I	---		---
C10	USB_SSRX2+	USB Super Speed Receive 2 +	DP-I	---		---
C11	GND	Power Ground	PWR GND	---		---
C12	USB_SSRX3-	USB Super Speed Receive 3 -	DP-I	---		---
C13	USB_SSRX3+	USB Super Speed Receive 3 +	DP-I	---		---
C14	GND	Power Ground	PWR GND	---		---
C15	DDI1_PAIR6+	Not Connected	nc	---		---
C16	DDI1_PAIR6-	Not Connected	nc	---		---
C17	RSVD	Reserved for future use	nc	---		---
C18	RSVD	Reserved for future use	nc	---		---
C19	PCIE_RX6+	PCI Express Lane 6 Receive +	DP-I	---		---
C20	PCIE_RX6-	PCI Express Lane 6 Receive -	DP-I	---		---
C21	GND	Power Ground	PWR GND	---		---
C22	PCIE_RX7+	PCI Express Lane 7 Receive +	DP-I	---		---
C23	PCIE_RX7-	PCI Express Lane 7 Receive -	DP-I	---		---
C24	DDI1_HPD	DDI1 Hotplug Detect	I-3.3	PD 100k		
C25	DDI1_PAIR4+	Not Connected	nc	---		---
C26	DDI1_PAIR4-	Not Connected	nc	---		---
C27	RSVD	Reserved for future use	nc	---		---
C28	RSVD	Reserved for future use	nc	---		---
C29	DDI1_PAIR5+	Not Connected	nc	---		---
C30	DDI1_PAIR5-	Not Connected	nc	---		---
C31	GND	Power Ground	PWR GND	---		---
C32	DDI2_CTRLCLK_AUX+	DDI2 CTRLCLK/AUX+	I/O-3.3	PD 100k		---
C33	DDI2_CTRLDATA_AUX-	DDI2 CTRLDATA/AUX-	I/O-3.3	PU 100k 3.3V (S0)		---

Pin	Signal	Description	Type	Termination		Comment
C34	DDI2_DDC_AUX_SEL	DDI2 DDC/AUX select	I-3.3	PD 1M		---
C35	RSVD	Reserved for future use	nc	---		---
C36	DDI3_CTRLCLK_AUX+	DDI3 CTRLCLK/AUX+	I/O-3.3	PD 100k		---
C37	DDI3_CTRLDATA_AUX-	DDI3 CTRLDATA/AUX-	I/O-3.3	PU 100k 3.3V (S0)		---
C38	DDI3_DDC_AUX_SEL	DDI3 DDC/AUX select	I-3.3	PD 1M		---
C39	DDI3_PAIR0+	DDI3 Pair 0 +	DP-O	---		---
C40	DDI3_PAIR0-	DDI3 Pair 0 -	DP-O	---		---
C41	GND	Power Ground	PWR GND	---		---
C42	DDI3_PAIR1+	DDI3 Pair 1 +	DP-O	---		---
C43	DDI3_PAIR1-	DDI3 Pair 1 -	DP-O	---		---
C44	DDI3_HPD	DDI3 Hotplug Detect	I-3.3	PD 100k		---
C45	RSVD	Reserved for future use	nc	---		---
C46	DDI3_PAIR2+	DDI3 Pair 2 +	DP-O	---		---
C47	DDI3_PAIR2-	DDI3 Pair 2 -	DP-O	---		---
C48	RSVD	Reserved for future use	nc	---		---
C49	DDI3_PAIR3+	DDI3 Pair 3 +	DP-O	---		---
C50	DDI3_PAIR3-	DDI3 Pair 3 -	DP-O	---		---
C51	GND	Power Ground	PWR GND	---		---
C52	PEG_RX0+	PEG Lane 0 Receive +	DP-I	---		---
C53	PEG_RX0-	PEG Lane 0 Receive -	DP-I	---		---
C54	TYPE0#	nc for type 6 module	nc	---		---
C55	PEG_RX1+	PEG Lane 1 Receive +	DP-I	---		---
C56	PEG_RX1-	PEG Lane 1 Receive -	DP-I	---		---
C57	TYPE1#	nc for type 6 module	nc	---		---
C58	PEG_RX2+	PEG Lane 2 Receive +	DP-I	---		---
C59	PEG_RX2-	PEG Lane 2 Receive -	DP-I	---		---
C60	GND	Power Ground	PWR GND	---		---
C61	PEG_RX3+	PEG Lane 3 Receive +	DP-I	---		---
C62	PEG_RX3-	PEG Lane 3 Receive -	DP-I	---		---
C63	RSVD	Reserved for future use	nc	---		---
C64	RSVD	Reserved for future use	nc	---		---
C65	PEG_RX4+	PEG Lane 4 Receive +	DP-I	---		---
C66	PEG_RX4-	PEG Lane 4 Receive -	DP-I	---		---
C67	RAPID_SHUTDOWN	Rapid Shutdown Trigger Input	nc	---		---
C68	PEG_RX5+	PEG Lane 5 Receive +	DP-I	---		---
C69	PEG_RX5-	PEG Lane 5 Receive -	DP-I	---		---

Pin	Signal	Description	Type	Termination		Comment
C70	GND	Power Ground	PWR GND	---		---
C71	PEG_RX6+	PEG Lane 6 Receive +	DP-I	---		---
C72	PEG_RX6-	PEG Lane 6 Receive -	DP-I	---		---
C73	GND	Power Ground	PWR GND	---		---
C74	PEG_RX7+	PEG Lane 7 Receive +	DP-I	---		---
C75	PEG_RX7-	PEG Lane 7 Receive -	DP-I	---		---
C76	GND	Power Ground	PWR GND	---		---
C77	RSVD	Reserved for future use	nc	---		---
C78	PEG_RX8+	PEG Lane 8 Receive +	DP-I	---		---
C79	PEG_RX8-	PEG Lane 8 Receive -	DP-I	---		---
C80	GND	Power Ground	PWR GND	---		---
C81	PEG_RX9+	PEG Lane 9 Receive +	DP-I	---		---
C82	PEG_RX9-	PEG Lane 9 Receive -	DP-I	---		---
C83	RSVD	Reserved for future use	nc	---		---
C84	GND	Power Ground	PWR GND	---		---
C85	PEG_RX10+	PEG Lane 10 Receive +	DP-I	---		---
C86	PEG_RX10-	PEG Lane 10 Receive -	DP-I	---		---
C87	GND	Power Ground	PWR GND	---		---
C88	PEG_RX11+	PEG Lane 11 Receive +	DP-I	---		---
C89	PEG_RX11-	PEG Lane 11 Receive -	DP-I	---		---
C90	GND	Power Ground	PWR GND	---		---
C91	PEG_RX12+	PEG Lane 12 Receive +	DP-I	---		---
C92	PEG_RX12-	PEG Lane 12 Receive -	DP-I	---		---
C93	GND	Power Ground	PWR GND	---		---
C94	PEG_RX13+	PEG Lane 13 Receive +	DP-I	---		---
C95	PEG_RX13-	PEG Lane 13 Receive -	DP-I	---		---
C96	GND	Power Ground	PWR GND	---		---
C97	RSVD	Reserved for future use	nc	---		---
C98	PEG_RX14+	PEG Lane 14 Receive +	DP-I	---		---
C99	PEG_RX14-	PEG Lane 14 Receive -	DP-I	---		---
C100	GND	Power Ground	PWR GND	---		---
C101	PEG_RX15+	PEG Lane 15 Receive +	DP-I	---		---
C102	PEG_RX15-	PEG Lane 15 Receive -	DP-I	---		---
C103	GND	Power Ground	PWR GND	---		---

Pin	Signal	Description	Type	Termination		Comment
C104	VCC_12V	Main Input Voltage (4.75-20V)	PWR 4.75-20V	---		---
C105	VCC_12V	Main Input Voltage (4.75-20V)	PWR 4.75-20V	---		---
C106	VCC_12V	Main Input Voltage (4.75-20V)	PWR 4.75-20V	---		---
C107	VCC_12V	Main Input Voltage (4.75-20V)	PWR 4.75-20V	---		---
C108	VCC_12V	Main Input Voltage (4.75-20V)	PWR 4.75-20V	---		---
C109	VCC_12V	Main Input Voltage (4.75-20V)	PWR 4.75-20V	---		---
C110	GND	Power Ground	PWR GND	---		---

+ and - Differential pair differentiator

5.2.4. Connector X1B Row D 1 - D 110

Table 54: Connector X1B Row D Pin Assignment (D1-D110)

Pin	Signal	Description	Type	Termination	Comment
D1	GND	Power Ground	PWR GND	---	---
D2	GND	Power Ground	PWR GND	---	---
D3	USB_SSTX0-	USB Super Speed Transmit 0 -	DP-O	---	---
D4	USB_SSTX0+	USB Super Speed Transmit 0 +	DP-O	---	---
D5	GND	Power Ground	PWR GND	---	---
D6	USB_SSTX1-	USB Super Speed Transmit 1 -	DP-O	---	---
D7	USB_SSTX1+	USB Super Speed Transmit 1 +	DP-O	---	---
D8	GND	Power Ground	PWR GND	---	---
D9	USB_SSTX2-	USB Super Speed Transmit 2 -	DP-O	---	---
D10	USB_SSTX2+	USB Super Speed Transmit 2 +	DP-O	---	---
D11	GND	Power Ground	PWR GND	---	---
D12	USB_SSTX3-	USB Super Speed Transmit 3 -	DP-O	---	---
D13	USB_SSTX3+	USB Super Speed Transmit 3 +	DP-O	---	---
D14	GND	Power Ground	PWR GND	---	---
D15	DDI1_CTRLCLK_AUX+	DDI1 CTRLCLK/AUX+	I/O-3.3	PD 100k	---
D16	DDI1_CTRLDATA_AUX-	DDI1 CTRLDATA/AUX-	I/O-3.3	PU 100k 3.3V (S0)	---
D17	RSVD	Reserved for future use	nc	---	---

Pin	Signal	Description	Type	Termination	Comment
D18	RSVD	Reserved for future use	nc	---	---
D19	PCIE_TX6+	PCI Express Lane 6 Transmit +	DP-O	---	---
D20	PCIE_TX6-	PCI Express Lane 6 Transmit -	DP-O	---	---
D21	GND	Power Ground	PWR GND	---	---
D22	PCIE_TX7+	PCI Express Lane 7 Transmit +	DP-O	---	---
D23	PCIE_TX7-	PCI Express Lane 7 Transmit -	DP-O	---	---
D24	RSVD	Reserved for future use	nc	---	---
D25	RSVD	Reserved for future use	nc	---	---
D26	DDI1_PAIR0+	DDI1 Pair 0 +	DP-O	---	---
D27	DDI1_PAIR0-	DDI1 Pair 0 -	DP-O	---	---
D28	RSVD	Reserved for future use	nc	---	---
D29	DDI1_PAIR1+	DDI1 Pair 1 +	DP-O	---	---
D30	DDI1_PAIR1-	DDI1 Pair 1 -	DP-O	---	---
D31	GND	Power Ground	PWR GND	---	---
D32	DDI1_PAIR2+	DDI1 Pair 2 +	DP-O	---	---
D33	DDI1_PAIR2-	DDI1 Pair 2 -	DP-O	---	---
D34	DDI1_DDC_AUX_SEL	DDI1 DDC/AUX select	I-3.3	PD 1M	---
D35	RSVD	Reserved for future use	nc	---	---
D36	DDI1_PAIR3+	DDI1 Pair 3 +	DP-O	---	---
D37	DDI1_PAIR3-	DDI1 Pair 3 -	DP-O	---	---
D38	RSVD	Reserved for future use	nc	---	---
D39	DDI2_PAIR0+	DDI2 Pair 0 +	DP-O	---	---
D40	DDI2_PAIR0-	DDI2 Pair 0 -	DP-O	---	---
D41	GND	Power Ground	PWR GND	---	---
D42	DDI2_PAIR1+	DDI2 Pair 1 +	DP-O	---	---
D43	DDI2_PAIR1-	DDI2 Pair 1 -	DP-O	---	---
D44	DDI2_HPD	DDI2 Hotplug Detect	I-3.3	PD 100k	---
D45	RSVD	Reserved for future use	nc	---	---
D46	DDI2_PAIR2+	DDI2 Pair 2 +	DP-O	---	---
D47	DDI2_PAIR2-	DDI2 Pair 2 -	DP-O	---	---
D48	RSVD	Reserved for future use	nc	---	---
D49	DDI2_PAIR3+	DDI2 Pair 3 +	DP-O	---	---
D50	DDI2_PAIR3-	DDI2 Pair 3 -	DP-O	---	---
D51	GND	Power Ground	PWR GND	---	---
D52	PEG_TX0+	PEG Lane 0 Transmit +	DP-O	---	---
D53	PEG_TX0-	PEG Lane 0 Transmit -	DP-O	---	---
D54	PEG_LANE_RV#	Not Connected	nc	---	---
D55	PEG_TX1+	PEG Lane 1 Transmit +	DP-O	---	---
D56	PEG_TX1-	PEG Lane 1 Transmit -	DP-O	---	---
D57	TYPE2#	GND for type 6 module	PWR	---	---
D58	PEG_TX2+	PEG Lane 2 Transmit +	DP-O	---	---
D59	PEG_TX2-	PEG Lane 2 Transmit -	DP-O	---	---

Pin	Signal	Description	Type	Termination	Comment
D60	GND	Power Ground	PWR GND	---	---
D61	PEG_TX3+	PEG Lane 3 Transmit +	DP-O	---	---
D62	PEG_TX3-	PEG Lane 3 Transmit -	DP-O	---	---
D63	RSVD	Reserved for future use	nc	---	---
D64	RSVD	Reserved for future use	nc	---	---
D65	PEG_TX4+	PEG Lane 4 Transmit +	DP-O	---	---
D66	PEG_TX4-	PEG Lane 4 Transmit -	DP-O	---	---
D67	GND	Power Ground	PWR GND	---	---
D68	PEG_TX5+	PEG Lane 5 Transmit +	DP-O	---	---
D69	PEG_TX5-	PEG Lane 5 Transmit -	DP-O	---	---
D70	GND	Power Ground	PWR GND	---	---
D71	PEG_TX6+	PEG Lane 6 Transmit +	DP-O	---	---
D72	PEG_TX6-	PEG Lane 6 Transmit -	DP-O	---	---
D73	GND	Power Ground	PWR GND	---	---
D74	PEG_TX7+	PEG Lane 7 Transmit +	DP-O	---	---
D75	PEG_TX7-	PEG Lane 7 Transmit -	DP-O	---	---
D76	GND	Power Ground	PWR GND	---	---
D77	RSVD	Reserved for future use	nc	---	---
D78	PEG_TX8+	PEG Lane 8 Transmit +	DP-O	---	---
D79	PEG_TX8-	PEG Lane 8 Transmit -	DP-O	---	---
D80	GND	Power Ground	PWR GND	---	---
D81	PEG_TX9+	PEG Lane 9 Transmit +	DP-O	---	---
D82	PEG_TX9-	PEG Lane 9 Transmit -	DP-O	---	---
D83	RSVD	Reserved for future use	nc	---	---
D84	GND	Power Ground	PWR GND	---	---
D85	PEG_TX10+	PEG Lane 10 Transmit +	nc	---	---
D86	PEG_TX10-	PEG Lane 10 Transmit -	nc	---	---
D87	GND	Power Ground	PWR GND	---	---
D88	PEG_TX11+	PEG Lane 11 Transmit +	DP-O	---	---
D89	PEG_TX11-	PEG Lane 11 Transmit -	DP-O	---	---
D90	GND	Power Ground	PWR GND	---	---
D91	PEG_TX12+	PEG Lane 12 Transmit +	DP-O	---	---
D92	PEG_TX12-	PEG Lane 12 Transmit -	DP-O	---	---
D93	GND	Power Ground	PWR GND	---	---
D94	PEG_TX13+	PEG Lane 13 Transmit +	DP-O	---	---
D95	PEG_TX13-	PEG Lane 13 Transmit -	DP-O	---	---
D96	GND	Power Ground	PWR GND	---	---
D97	RSVD	Reserved for future use	nc	---	---
D98	PEG_TX14+	PEG Lane 14 Transmit +	DP-O	---	---
D99	PEG_TX14-	PEG Lane 14 Transmit -	DP-O	---	---
D100	GND	Power Ground	PWR GND	---	---
D101	PEG_TX15+	PEG Lane 15 Transmit +	DP-O	---	---

Pin	Signal	Description	Type	Termination	Comment
D102	PEG_TX15-	PEG Lane 15 Transmit -	DP-O	---	---
D103	GND	Power Ground	PWR GND	---	---
D104	VCC_12V	Main Input Voltage (4.75-20V)	PWR 4.75-20V	---	---
D105	VCC_12V	Main Input Voltage (4.75-20V)	PWR 4.75-20V	---	---
D106	VCC_12V	Main Input Voltage (4.75-20V)	PWR 4.75-20V	---	---
D107	VCC_12V	Main Input Voltage (4.75-20V)	PWR 4.75-20V	---	---
D108	VCC_12V	Main Input Voltage (4.75-20V)	PWR 4.75-20V	---	---
D109	VCC_12V	Main Input Voltage (4.75-20V)	PWR 4.75-20V	---	---
D110	GND	Power Ground	PWR GND	---	---

+ and - Differential pair differentiator

6/ Maintenance

6.1. Blue Screen after BIOS Update

After updating the BIOS a previously installed Windows 10 does not start anymore and runs into a blue screen. Under 'Chipset > PCH-IO Configuration -> SATA and RST configuration > SATA mode selection' the user can select whether to use SATA in a normal 'AHCI' mode or as 'Intel RST Premium With IntelOptane System Acceleration'. Default setting is 'AHCI'. Missing this will cause Windows 10 to refuse to start showing a bluescreen containing the message 'Inaccessible Boot Device'.

If this value is being changed before Windows installation it has to be changed again after a BIOS update prior to Windows start. Otherwise next Windows start fails with a Blue Screen (BSOD). Now it seems that some Win driver installation changes this setting automatically so the user is not aware of the change that finally has gone lost through the BIOS update.

7/ uEFI BIOS

7.1. Starting the uEFI BIOS

The COMe-bCL6 is provided with a JUMPtec-customized, pre-installed and configured version of AMI Aptio ® V uEFI BIOS based on the Unified Extensible Firmware Interface (uEFI) specification and the Intel® Platform Innovation Framework for EFI. This uEFI BIOS provides a variety of new and enhanced functions specifically tailored to the hardware features of the COMe-bCL6.

The BIOS version covered in this document might not be the latest version. The latest version might have certain differences to the BIOS options and features described in this chapter.

Register for the EMD Customer Section to get access to BIOS downloads and PCN service.

The uEFI BIOS comes with a Setup program that provides quick and easy access to the individual function settings for control or modification of the uEFI BIOS configuration. The Setup program allows for access to various menus that provide functions or access to sub-menus with further specific functions of their own.

To start the uEFI BIOS Setup program, follow the steps below:

1. Power on the board.
2. Wait until the first characters appear on the screen (POST messages or splash screen).
3. Press the <DEL> key.
4. If the uEFI BIOS is password-protected, a request for password will appear. Enter either the User Password or the Supervisor Password (see Chapter 0), press <RETURN>, and proceed with step 5.
5. A Setup menu appears.

The COMe-bCL6 uEFI BIOS Setup program uses a hot key navigation system. The hot key legend bar is located at the bottom of the Setup screens. The following table provides a list of navigation hot keys available in the legend bar.

Table 55: Navigation Hot Keys Available in the Legend Bar

Sub-screen	Description
<F1>	<F1> key invokes the General Help window
<->	<Minus> key selects the next lower value within a field
<+>	<Plus> key selects the next higher value within a field
<F2>	<F2> key loads previous values
<F3>	<F3> key loads optimized defaults
<F4>	<F4> key Saves and Exits
<→> or <←>	<Left/Right> arrows selects major Setup menus on menu bar, for example, Main or Advanced
<↑> or <↓>	<Up/Down> arrows select fields in the current menu, for example, Setup function or sub-screen
<ESC>	<ESC> key exits a major Setup menu and enters the Exit Setup menu Pressing the <ESC> key in a sub-menu displays the next higher menu level
<RETURN>	<RETURN> key executes a command or selects a submenu

7.2. Setup Menus

The Setup utility features menus listed in the selection bar at the top of the screen:

- Main
- Advanced
- Chipset
- Security
- Boot
- Save & Exit

The left and right arrow keys select the Setup menus. The currently active menu and the currently active uEFI BIOS Setup item are highlighted in white.

Each Setup menu provides two main frames. The left frame displays all available functions. Configurable functions are displayed in blue. Functions displayed in grey provide information about the status or the operational configuration. The right frame displays an Item Specific Help window providing an explanation of the respective function.

7.2.1. Main Setup Menu

On entering the uEFI BIOS the Setup program displays the Main Setup menu. This screen lists the Main Setup menu sub-screens and provides basic system information as well as functions for setting the system language, time and date.

Figure 8: Main Setup Menu

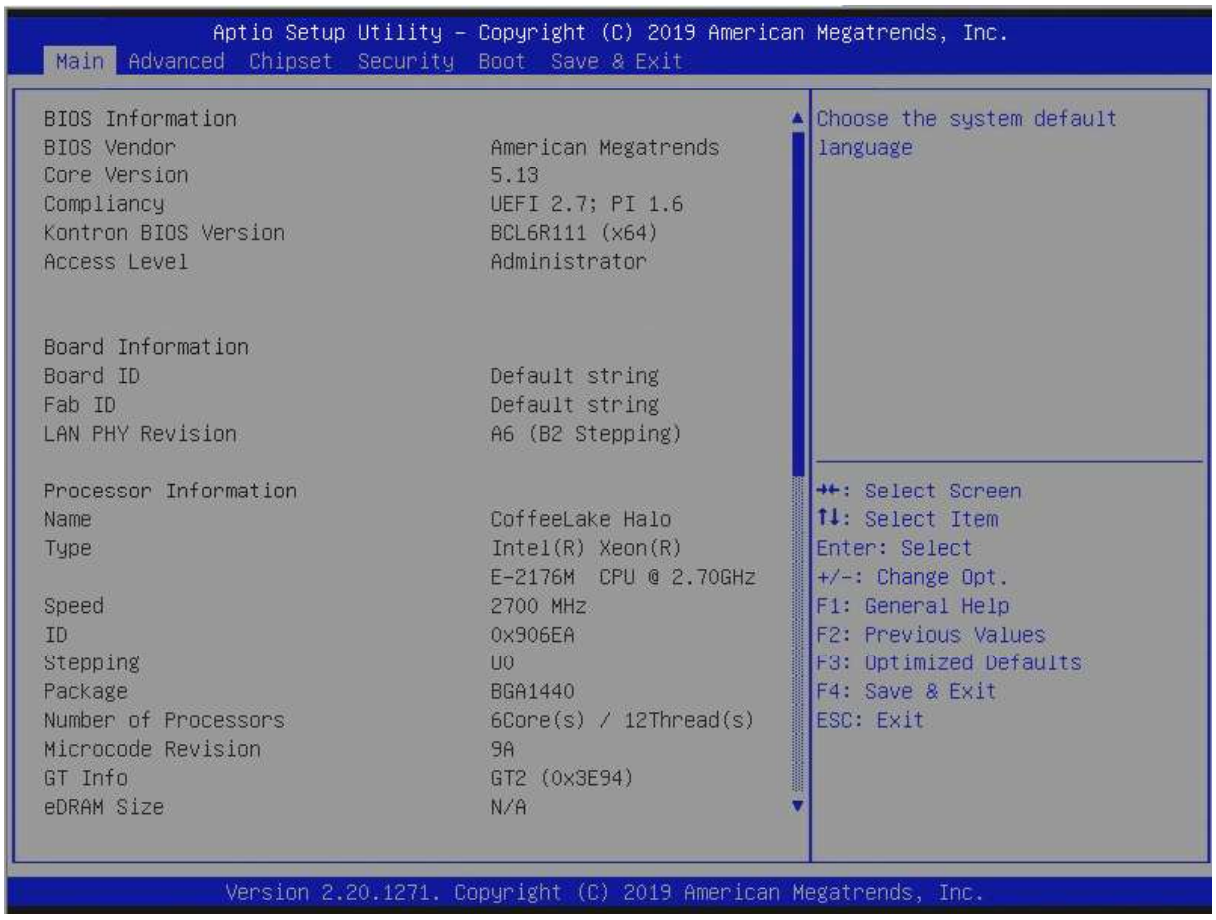


Table 56: Main Setup Menu Sub-screens and Functions

Sub-screen	Description
BIOS Information	Read only field Displays information about the BIOS system Vendor, Core version, Compliancy, JUMPtec BIOS Version, and Access level
Board Information	Read only field Board/Fab ID, LAN PHY Revision
Processor Information	Read only field Displays information about the CPU Name, Type, Speed, Processor ID, Stepping, Number of Processors, Microcode Version, and GT Info, ,
Memory Version	Read only field Displays information about eDRAM Size, IGFX VBIOS/IGFX GOP/Memory RC Version, Total memory and Memory Frequency

Sub-screen	Description
PCH Information	Read only field Displays information about the PCH Name, PCH SKU, Stepping, and LAN PHY Revision
ME FW	Read only field ME Firmware Version, ME Firmware Consumer SKU
System language	Selects System language
System Date	Displays System Date
System Time	Displays System Time

7.2.2. Advanced Setup Menu

The Advanced Setup menu provides sub-screens and second level sub-screens with functions, for advanced configuration and JUMPtec specific configurations.

NOTICE Setting items, on this screen, to incorrect values may cause system malfunctions.

Figure 9: Avanced Setup Menu

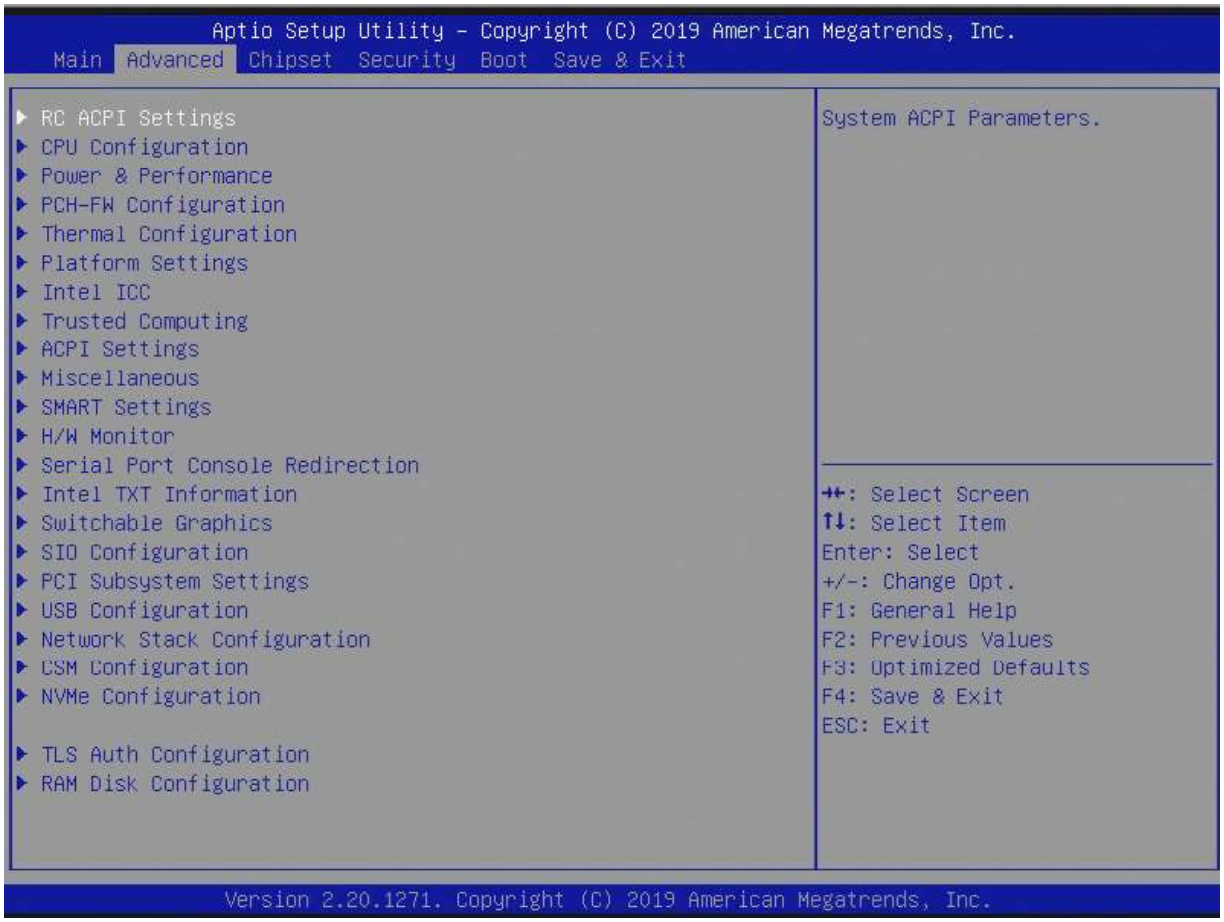


Table 57: Advanced Setup menu Sub-screens and Functions

Sub-Screen	Function	Second level Sub-Screen / Description
RC ACPI	PTID Support	**Enable**/Disable
	PECI Access Method	Direct I/O
	Native PCIE Enable	**Enable**/Disable
	Native ASPM	Auto
	Wake System from S5	Enable/**Disable**
	ACPI Debug	Enable/**Disable**
	Low Power S0 Idle Capability	Enable/**Disable**
	PCI Delay Optimization	Enable/**Disable**

Sub-Screen	Function	Second level Sub-Screen / Description	
	MSI enabled	**Enable**/Disable	
CPU Configuration	C6DRAM	**Enable**/Disable	
	Software Guard Extensions (SGX)	Software Controlled	
	Select Owner EPOCH input type	No Change in Owner EPOCHs	
	CPU Flex Ratio Override	Enable/**Disable**	
	Intel Virtual Technology>	**Enable**/Disable	
	Active Processor Cores>	All	
	Hyper Threading>	**Enable**/Disable	
	BIST	Enable/**Disable**	
Power & Performance	CPU Power Management Control	Boot Performance Mode	Max Non-Turbo Performance
		Intel SpeedStep	**Enable**/Disable
		Intel Speed ShiftTechnology	**Enable**/Disable
		Turbo Mode	**Enable**/Disable
		View/Configure Turbo Options	
		Config TDP Configurations	
		Platform PL1 Enable	Enable/**Disable**
		Platform PL2 Enable	Enable/**Disable**
		Platform PL4 Override	**Enable**/Disable
		Platform PL4 Power	0
		Platform PL4 Lock	**Enable**/Disable
		C states	**Enable**/Disable
		Package C State List	**Auto**
	GT Power Management Control	RC6 (Render Standby)	**Enable**/Disable
		Maximum GT frequency	**Default Max Frequency**
		Disable Turbo GT frequency	Enable/**Disable**
PCH-FW Configuration	ME State	**Enable**/Disable	
	Firmware Update Configuration	ME FW Image Re-Flash	Enable/**Disable**
		Local FW Update	**Enable**/Disable
	PTT Configuration	TPM Device Selection	dTPM/**PTT**
Thermal Configuration	CPU Thermal Configuration	DTS SMM	Enable/**Disable**
		TCC Activation Offset	0
		Disable PROCHOT# Output	**Enable**/Disable
	Platform Thermal Configuration	Automatic Thermal Reporting	Enable/**Disable**
		Critical Trip Point	119 C (POR)
		Passive Trip Point	95 C
		Passive TC1 value	1
		Passive TC2 value	5

Sub-Screen	Function	Second level Sub-Screen / Description	
		Passive TSP value	10
		Passive Trip Points	Enable/**Disable**
		Critical Trip Point	**Enable**/Disable
Platform Settings	System Time and Alarm Source	**ACPI Time and Alarm Device**/Legacy RTC	
Intel ICC	ICC/OC Watchdog Timer	Enable/**Disable**	
	ICC Profile	0	
	ICC PLL Shutdown	**Enable**/Disable	
Trusted Computing	Security Device Support	**Enable**/Disable	
	SHA-1 PCR Bank	**Enable**/Disable	
	SHA256 PCR Bank	**Enable**/Disable	
	Pending Operation	**None**	
	Platform Hierarchy	**Enable**/Disable	
	Storage Hierarchy	**Enable**/Disable	
	Endorsement Hierarchy	**Enable**/Disable	
	TPM 2.0 UEFI Spec Version	**TCG_2**	
	Physical Presence Spec Version	**1.3**	
	Device Select	**Auto**	
ACPI settings	Enable ACPI Auto Configuration>	Enable/**disable**	
	Enable Hibernation>	**Enable**/disable	
	ACPI Sleep State	S3	
	Lock Legacy Resources>	Enable/**disable**	
	S3 Video Repost>	Enable/**disable**	
Miscellaneous	Generic LPC Decode Ranges	Generic LPC Decode 1	Enable/**Disable**
	Watchdog	Auto-Reload	Enable/**Disable**
		Global Lock	Enable/**Disable**
		Stage 1 Mode	Enable/**Disable**
	Reset Button Behavior	Chipset Reset	
	I2C Speed	200	
	Onboard I2C Mode	Multimaster	
	Lid Switch Mode	Enable/**Disable**	
	Sleep Button Mode	Enable/**Disable**	
	ACPI temperature polling	**Enable**/Disable	

Sub-Screen	Function	Second level Sub-Screen / Description
	T200 temperature polling	30
	Control COMe GPIOs in BIOS	Enable/**Disable**
	GPIO IRQ-/ I2C IRQ OS assigned	**Enable**/Disable
SMART Settings	SMART Self Test	Enable/**Disable**
H/W Monitor	CPU Fan: Fan Control	Auto
	Fan Pulse	2
	Fan Trip Point	50
	Trip Point Speed	50
	Reference Temperature	CPU Temperature
	External Fan: Fan Control	Auto
	Fan Pulse	2
	Fan Trip Point	50
	Trip Point Speed	50
	Reference Temperature	CPU Temperature
Serial Port Console Redirection	COM0 Console Redirection	Enable/**Disable**
	COM1 Console Redirection	Enable/**Disable**
	Legacy Console Redirection	Redirection COM Port [**COM0**]
		Resolution [**80x24**]
		Redirecion After POST [**Always Enable**]
	Console Redirection	Enable/**Disable**
Intel TXT Inf.		
Switch. Graphics		
SIO Configuration	Serial Port 0	
	Serial Port 1	
PCI Subsystem Settings	BME DMA Mitigation	Enable/**Disable**
USB Configuration	Legacy USB Support	**Enable**/Disable
	XHCI Hand-Off	**Enable**/Disable
	USB Mass Storage Driver Support	**Enable**/Disable
	USB transfer time-out	20 sec
	Device reset time-out	20 sec
	Device power-up delay	Auto
Network Stack	Network Stack	Enable/**Disable**
CSM Configuration	CSM Support	Enable/**Disable**

Sub-Screen	Function	Second level Sub-Screen / Description
TLS Auth Configuration	Server CA Configuration	Enroll Cert/Delete Cert
	Client Cert Configuration	
RAM Disk Configuration	Disk Memory Type	**Boot Service Data**/Reserved
	Create raw	
	Create from file	
	Remove selected RAM disks	

NOTICE

Additional Watchdog Information

The COMe-bCL6 provides a two-staged watchdog with:

Programmable stages to trigger different actions - If one stage is disabled, then the next stage is also disabled.

Common actions for a watchdog trigger events **'Delay', 'Reset' and 'Watchdog signal only'**

CPLD code allows for triggering NMI or SCI. This needs programming of a predefined action inside the BIOS and therefore can only be used in a customized BIOS solution.

Timeouts that can be set to eight different fixed values between 1 second and 30 minutes.

NOTICE

Additional Information: External Fan

An external fan can be connected to baseboard. The external fan's control lines are routed via the COMe connector.

⚠WARNING

Additional SIO Information

Logical Devices state on the left side of the control reflects the current logical device state. Changes made during the setup session are shown after restarting the system.

The SIO Configuration menu enables all available serial interfaces to be configured. The module-based serial interfaces always appear as COM1 and COM2. COM 1 and COM 2 can be treated as 16550-compatible legacy COM interfaces at the standard I/O addresses and are based in the on-module CPLD. Note: Hardware flow control is not supported.

Optionally, If the baseboard contains an activated SuperIO of the type Winbond 83627, then its serial interfaces are added to the system as COM3 and COM4. COM3 and COM4 IRQ and I/O addresses are configurable in this menu, too.

Although the chipset internal COMs are not supported due to technical constraints their driver must be installed. Installing the driver does not mean that these serial interfaces are useable.

NOTICE

Additional CSM Information

Compatibility Support Module (CSM) configuration is important for legacy operating systems

By default, CSM is disabled for modern OS such as Windows 8, 10 and Linux.

If a legacy OS is used or a Windows or Linux system is run in legacy mode then this menu allows for detailed option settings.

Note, a change in settings only come into effect after the next restart. Therefore, to be able to use the actualized settings, it is recommended to save and exit setup and re-enter.

The 'Optional ROM Execution' settings require special care. Any OS using an INT10 based display output needs the 'Video' option set to 'Legacy', in the same way that PXE boot needs 'Network' 'Optional ROM' to be set to 'Legacy'.

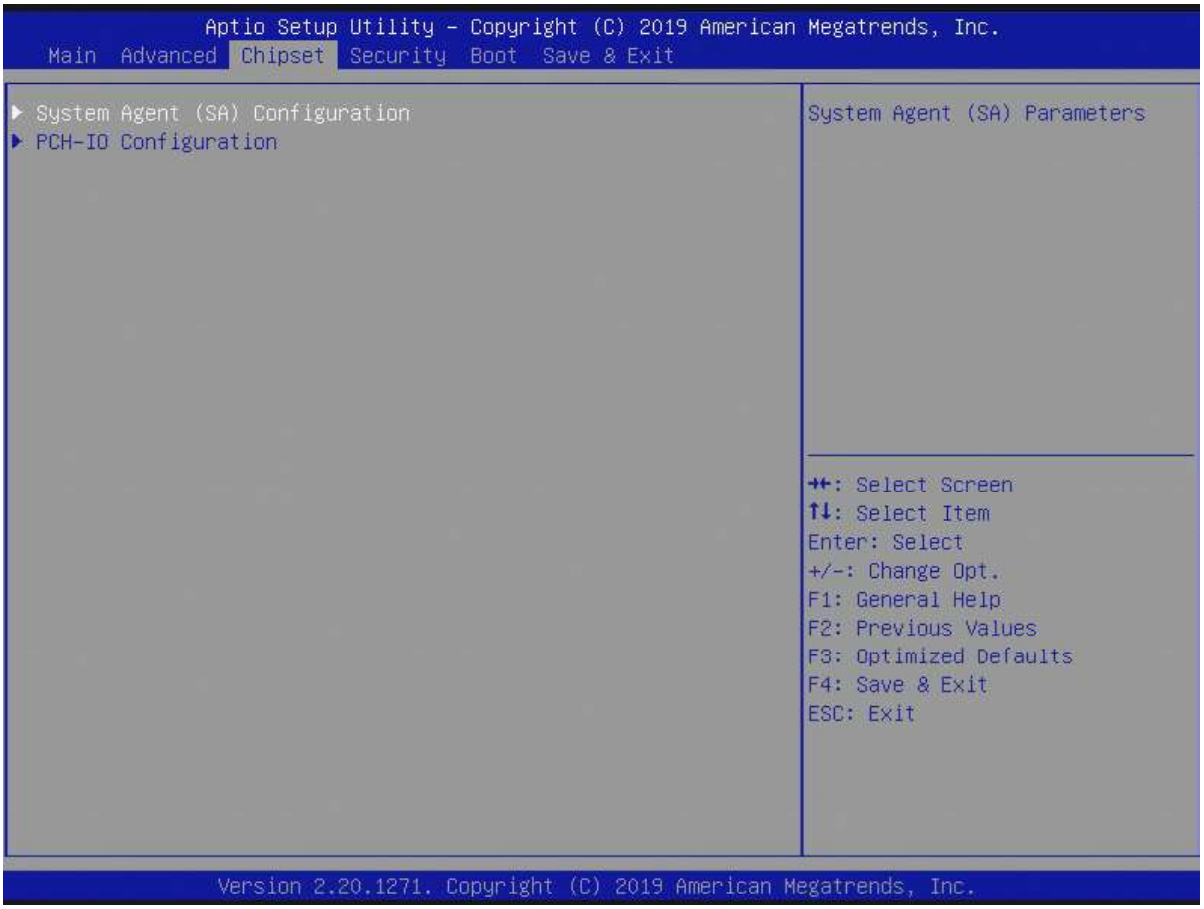
7.2.3. Chipset Setup Menu

On entering the Chipset Setup menu, the screen lists two sub-screen options:

- System Agent
- PCH-IO

Entering the System Agent Configuration and PCH-IO Configuration sub-screens provides basic system information and possible functions for these configurations.

Figure 10: Chipset Setup Menu



7.2.3.1. Chipset: System Agent Configuration

Table 58: Chipset: System Agent Configuration Sub-screens and Functions

Function	Second level Sub-Screen / Description		
Memory Configuration	Memory Test on Warm Boot	**Enable**/Disable	
	Maximum Memory Frequency	Auto	
	Max TOLUD	Dynamic	
Graphics Configuration	Skip Scanning Slots for External GfX Card	Enable/**Disable**	
	Primary Display	Auto	
	Select PCIE Card	Auto	
	External Gfx Card Primary Display Configuration		
	Internal Graphics	Auto	
	GTT Size	8 MB	
	Aperture Size	256 MB	
	DVMT Pre-Allocated	32 M	
	DVMT Total Gfx Mem	256 M	
	IGD Configuration	IGD Boot Type	Auto
		LFD Panel Type	LVDS
		Backlight Control	PWM
		PWM Frequency	200 Hz
		Backlight Value	128
		LVDS Clock Center Spreading	no Spreading
		EFP1 Type	DP with HDMI/DVI
		EFP1 LSPCON	Enable/**Disable**
		EFP2 Type	DP with HDMI/DVI
		EFP2 LSPCON	Enable/**Disable**
		EFP3 Type	DP with HDMI/DVI
		EFP3 LSPCON	Enable/**Disable**
		Mode Persistence	Enable/**Disable**
		Center Mode	Enable/**Disable**
PEG Port Configuration	Enable Root Port	Auto	
	Max Link Speed	Auto	
	PEG0 Slot Power Limit Value	75	

Function	Second level Sub-Screen / Description	
	PEG0 Slot Power Limit Scale	1.0x
	PEG0 Physical Slot Number	1
	PEG Port Feature Configuration	Detect Non Compliance Device [Enable/**Disable**]
		PCIe Spread Spectrum Clocking [**Enable**/Disable]
PEG Width Configuration	PEG Width Configuration	1x16
Stop Grant Configuration	Auto	
VT-d	**Enable**/Disable	

NOTICE

Additional Information for LCD Control

The bCL6 allows three different displays to be connected where one display is LVDS and the others are DisplayPort/HDMI/DVI connectors on the baseboard.

If connected to a display LVDS is always the first in the row of active devices. By using different methods such as EDID data (V1.3 or 1.4), DiID (DisplayID) or Kontron's JILI data, it is possible, in most cases, to show a valid picture on a newly connected LVDS panel. However, in special cases the panel size can be chosen manually from a list.

If the 'Auto' setting does not match the needs then it is also possible to manually determine which display to use. In this case, there is a setting for first display and secondary display. If one of them is LFP, then LFP options are also available.

7.2.3.2. Chipset > PCH-IO Configuration

Table 59: Chipset Set > PCH-IO Configuration Sub-screens and Functions

Function	Second level Sub-Screen / Description		
PCI Express Configuration	Port8xh Decode	Enable/**Disable**	
	PCI-USB Glitch W/A	Enable/**Disable**	
	PCIe Root Port 9	PCI Expr. Root Port 9	**Enable**/Disable
		Connection Type	Slot
		ASPM8	Auto
		PME SCI	**Enable**/Disable
		Hot Plug	Enable/**Disable**
		PCIe Speed	Auto
		Detect Timeout	0
		Extra Bus Reserved	0
		Reserved Memory	10
		Reserved I/O	4

Function	Second level Sub-Screen / Description		
	PCIe Root Port 13 (COMe Lane 4) PCIe Root Port 14 (COMe Lane 5) PCIe Root Port 15 (COMe Lane 6) PCIe Root Port 16 (COMe Lane 7) PCIe Root Port 21 (COMe Lane 0) PCIe Root Port 22 (COMe Lane 1) PCIe Root Port 23 (COMe Lane 2) PCIe Root Port 24 (COMe Lane 3)	PCI Expr. Root Port 13, 14, 15, 16, 21, 22, 23, 24	**Enable**/Disable
		Connection Type	Slot
		ASPM8	Auto
		PME SCI	**Enable**/Disable
		Hot Plug	Enable/**Disable**
		PCIe Speed	Auto
		Detect Timeout	0
		Extra Bus Reserved	0
		Reserved Memory	10
		Reserved I/O	4
SATA and RST Configuration	SATA Controller	**Enable**/Disable	
	SATA Mode Selection	AHCI	
	Software Feature Mask Configuration	HDD Unlock	**Enable**/Disable
		LED Locate	**Enable**/Disable
	Serial ATA Port 0, 1, 2, 3	Port 0, 1, 2, 3	**Enable**/Disable
		External	Enable/**Disable**
		Spin Up Device	Enable/**Disable**
		SATA Device Type	Hard Disk Drive
USB Configuration	xDCI Support	Enable/**Disable**	
	USB Overcurrent	**Enable**/Disable	
	USB Overcurrent Lock	**Enable**/Disable	
	USB Port Disable Override	Enable/**Disable**	
Security Configuration	RTC Memory Lock	**Enable**/Disable	
	BIOS Lock	**Enable**/Disable	
	Force unlock on all GPIO pads	Enable/**Disable**	
HD Audio Subsystem Configuration	HD Audio	**Enable**/Disable	
SerialIO Configuration	SPIO Controller	Enable/**Disable**	
PCH LAN Controller	**Enable**/Disable		
Wake on LAN	**Enable**/Disable		
Serial IRQ Mode>	Continuous		
State after G3	S0 State		

Function	Second level Sub-Screen / Description		
Port 80h Redirection	LPC Bus		
Enhance Port 80h LPC Decoding	Enable/**Disable**		
Enable TCO Timer	Enable/**Disable**		
PCIe P11 SSC	[Auto, **0.0%**, ...]		
SPD Write Disable	True		

NOTICE

Additional Information for PCI port
The PCIe menu refers to the different PCIe lanes using their chipset based numbers. For every lane, the number used on the COMe connector is mentioned. Take care to select the PCIe lane you require as numbering varies strongly.
The standard layout for PCIe consists of 8 PCIe 1x lanes.
Other layouts may be programmed by flashing a different descriptor to the Intel firmware on theBIOS SPI flash. Contact JUMPtec Support if you require different PCIe layout with your project.

7.2.4. Security Setup Menu

The Security Setup menu provides information about the passwords and functions for specifying the security settings. The passwords are case-sensitive.

Figure 11: Security Setup Menu

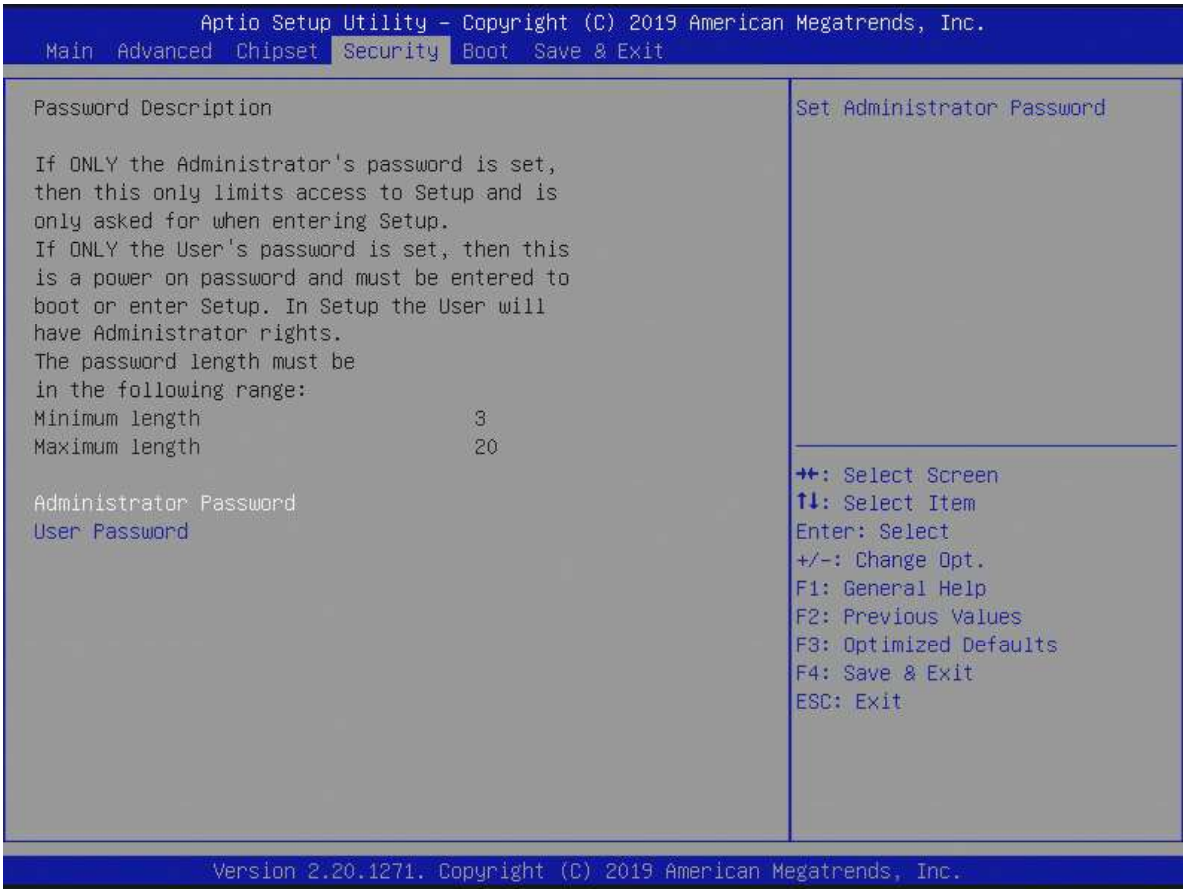


Table 60: Security Setup Menu Functions

Function	Description
Administrator Password	Sets administrator password
User Password	Sets user password

If only the administrator's password is set, then only access to setup is limited. The password is only entered when entering setup.

If only the user's password is set, then the password is a power on password and must be entered to boot or enter setup. Within the setup menu the user has administrator rights.

Password length requirements are maximum length 20 and minimum length 3.

7.2.4.1. Remember the Password

It is highly recommended to keep a record of all passwords in a safe place. Forgotten passwords results in the user being locked out of the system.

If the system cannot be booted because the User Password or the Supervisor Password are not known, see Chapter 7.5 Firmware Update for information about clearing the uEFI BIOS settings, or contact JUMPtec Support for further assistance.

HDD security passwords cannot be cleared using the above method.

7.2.5. Boot Setup Menu

The Boot Setup menu lists dynamically generated boot device priority order.

Figure 12: Boot Setup Menu

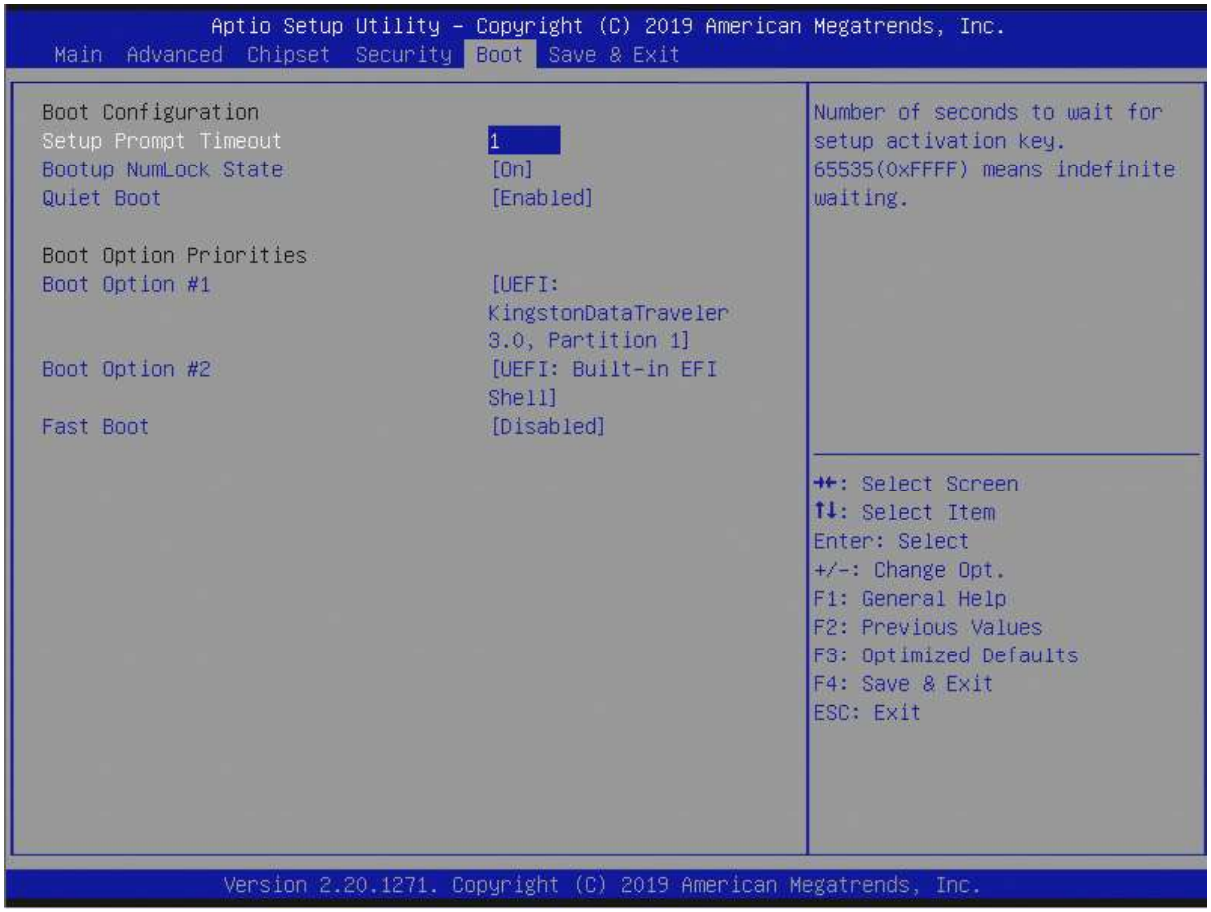


Table 61: Boot Setup Menu Functions

Function	Description
Setup Prompt Timeout	Displays number of seconds that the firmware waits before initiating the original default boot selection
Bootup NumLock State	Selects keyboard NumLock state
Quiet Boot	Enables\disables Quiet Boot
Boot Option #1	Sets the system boot order
Fast Boot	Enables/disables boot with initialization of a minimal set of devices required to launch active boot option This has no effect for BBS boot options.
New Boot Option Policy	Controls placement of newly detected UEFI boot options

7.2.6. Save and Exit Setup Menu

The Save and Exit Setup menu provides functions for handling changes made to the uEFI BIOS settings and exiting of the Setup program.

Figure 13: Save and Exit Setup Menu

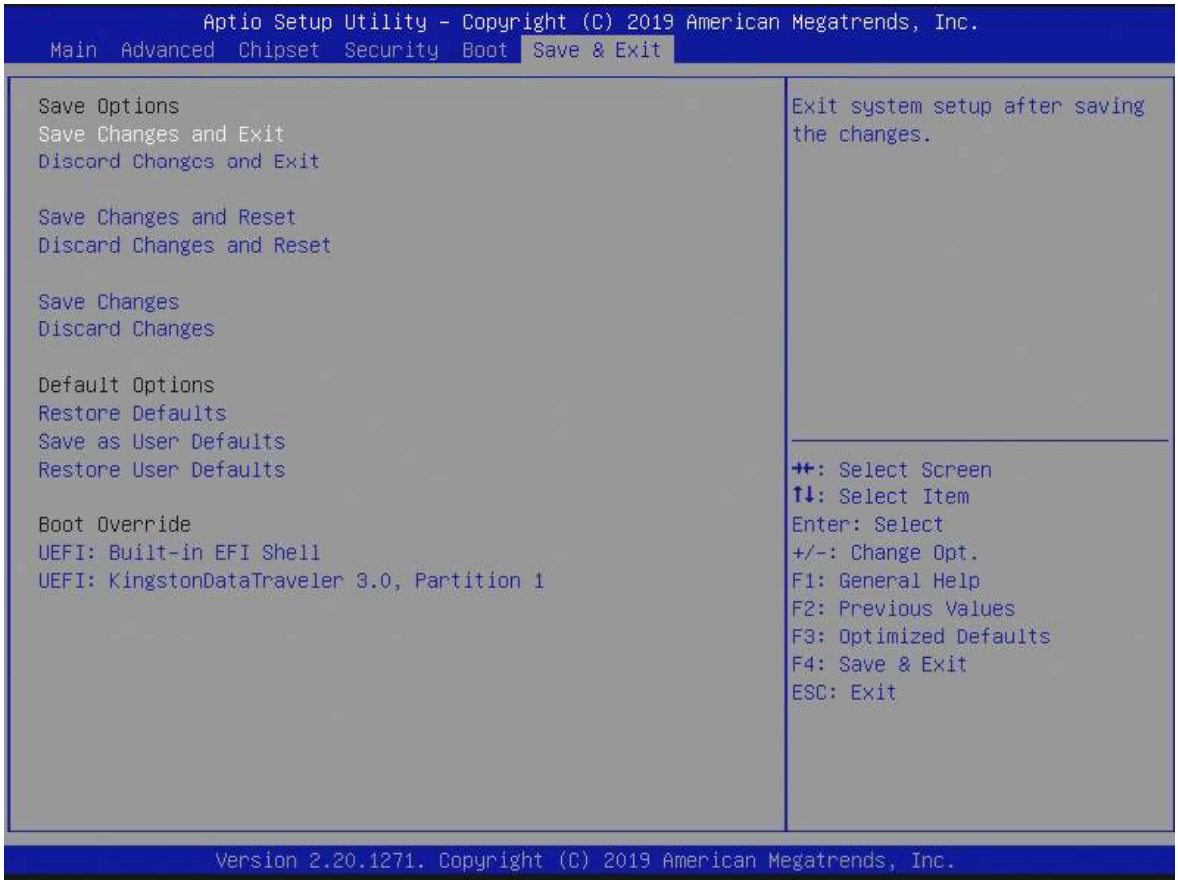


Table 62: Save and Exit Setup Menu Functions

Function	Description
Save Changes and Exit>	Exits system after saving changes
Discard Changes and Exit>	Exits system setup without saving changes
Save Changes and Reset>	Resets system after saving changes
Discard Changes and Reset>	Resets system setup without saving changes
Save Changes>	Saves changes made so far for any setup options
Discard Changes>	Discards changes made so far for any setup options
Restore Defaults>	Restores/loads standard default values for all setup options
Save as User Defaults>	Saves changes made so far as user defaults
Restore User Defaults>	Restores user defaults to all setup options
UEFI: Built-in EFI shell>	Attempts to launch the built in EFI Shell
UEFI: KingstonDataTraveler 3.0 >	Attempts to launch EFI Shell application (Shell.efi) from one of the available file system devices

7.3. The uEFI Shell

The JUMPtec uEFI BIOS features a built-in and enhanced version of the uEFI Shell. For a detailed description of the available standard shell scripting, refer to the EFI Shell User Guide. For a detailed description of the available standard shell commands, refer to the EFI Shell Command Manual. Both documents can be downloaded from the EFI and Framework Open Source Community homepage (http://sourceforge.net/projects/efi-shell/files/documents/).

JUMPtec uEFI BIOS does not provide all shell commands described in the EFI Shell Command Manual.

7.3.1. Basic Operation of the uEFI Shell

The uEFI Shell forms an entry into the uEFI boot order and is the first boot option by default.

7.3.1.1. Entering the uEFI Shell

To enter the uEFI Shell, follow the steps below:

1. Power on the board.
2. Press the <F7> key (instead of <DEL>) to display a choice of boot devices.
3. Choose 'UEFI: Built-in EFI shell'.

```
        UEFI Interactive Shell v2.2
        EDKII / JUMPtec add-on v0.1
         UEFI v2.70 (American Megatrends, 0x0005000D)
         Mapping table:
                 FS0:     Alias(s):HD0f0b:;BLK1:
                          PciRoot(0x0)/Pci(0x14,0x0)/USB(0x5,0x0)/HD(1,MBR,0x0008131B,0x1,0x6C7ff)
                 BLK0:    Alias(s):
                          PciRoot(0x0)/Pci(0x14,0x0)/USB(0x5,0x0)
```

4. Press the ESC key within 5 seconds to skip startup.nsh, and any other key to continue.
5. The output produced by the device-mapping table can vary depending on the board's configuration.
6. If the ESC key is pressed before the 5 second timeout elapses, the shell prompt is shown:

```
        Shell>
```

7.3.1.2. Exiting the uEFI Shell

To exit the uEFI Shell, follow one of the steps below:

1. Use the **exit** uEFI Shell command to select the boot device, in the Boot menu, for the OS to boot from.
2. Reset the board using the **reset** uEFI Shell command.

7.4. uEFI Shell Scripting

7.4.1. Startup Scripting

If the ESC key is not pressed and the timeout has run out then the uEFI Shell tries to execute some startup scripts automatically. It searches for scripts and executes them in the following order:

1. Initially searches for JUMPtec flash-stored startup script.
2. If there is no JUMPtec flash-stored startup script present then the uEFI-specified **`startup.nsh`** script is used. This script must be located on the root of any of the attached FAT formatted disk drive.
3. If none of the startup scripts are present or the startup script terminates then the default boot order is continued.

7.4.2. Create a Startup Script

Startup scripts can be created using the uEFI Shell built-in editor **edit** or under any OS with a plain text editor of your choice. To create a startup shell script, simply save the script on the root of any FAT-formatted drive attached to the system. To copy the startup script to the flash, use the **kBootScript** uEFI Shell command.

In case there is no mass storage device attached, the startup script can be generated in a RAM disk and stored in the SPI boot flash using the **kRamdisk** uEFI Shell command.

7.4.3. Examples of Startup Scripts

7.4.3.1. Execute Shell Script on Other Harddrive

This example (**`startup.nsh)`** executes the shell script named **`bootme.nsh`** located in the root of the first detected disc drive (**`fs0`**).

```
fs0:
bootme.nsh
```

7.5. Firmware Update

Firmware updates are typically delivered as a ZIP archive containing only the firmware images. The content of the archive with the directory structure must be copied onto a data storage device with FAT partition.

7.5.1.1. Updating Procedure

BIOS can be updated with the Intel tool fpt.efi using the procedure below:

1. Copy these files to an USB stick.

   flash.nsh (if available)

   fpt.efi

   fparts.txt

   bCL6r<xxx>.bin (where xxx stands for the version #)
2. Start the system into setup (see Chapter 7.1).
3. Change the BIOS option:

   Chipset > PCH-IO Configuration > BIOS Security Configuration > BIOS Lock > Disabled
4. Save and Exit the BIOS setup.
5. On the next start, boot into shell (see Chapter 7.5.1.1).
6. Change to the drive representing the USB stick

   ```
   fsx:   (x = 0,1,2,etc. represents the USB stick)
   ```

   and then change to the directory where you copied the flash tool.

   ```
   cd <your_directory>
   ```
7. Start flash.nsh (if available) OR enter

   ```
   fpt -SAVEMAC -F BCL6R<xxx>.bin
   ```
8. Wait until flashing is successful and then power cycle the board.

Do not switch off the power during the flash process! Doing so leaves your module unrecoverable.

Changes under point 3 are only effective during the first boot after the changes were applied. If you fail to flash during the next boot then you might have to repeat steps under point 3.

Do not forget to apply –SAVEMAC. If SAVEMAC is not applied then your system will lose its system MAC address. If the MAC address is accidentally deleted, contact JUMPtec Support.

8/ Technical Support

For technical support contact our Support department:

- E-mail: support@JUMPtec.com
- Phone: +49-821-4086-888

Make sure you have the following information available when you call:

- Product ID Number (PN),
- Serial Number (SN)
- Module's revision
- Operating System and Kernel/Build version
- Software modifications
- Addition connected hardware/full description of hardware set up

Be ready to explain the nature of your problem to the service technician.

The serial number can be found on the Type Label, located on the product's rear side.

8.1. Warranty

Due to their limited service life, parts that by their nature are subject to a particularly high degree of wear (wearing parts) are excluded from the warranty beyond that provided by law. This applies to the CMOS battery, for example.

If there is a protection label on your product, then the warranty is lost if the product is opened.

8.2. Returning Defective Merchandise

All equipment returned to JUMPtec must have a Return of Material Authorization (RMA) number assigned exclusively by JUMPtec cannot be held responsible for any loss or damage caused to the equipment received without an RMA number. The buyer accepts responsibility for all freight charges for the return of goods to JUMPtec ´s designated facility. JUMPtec will pay the return freight charges back to the buyer's location in the event that the equipment is repaired or replaced within the stipulated warranty period. Follow these steps before returning any product to JUMPtec.

1. Visit the RMA Information website:
   http://www.congatec.com/support-and-services/support/rma-information

   Download the RMA Request sheet for JUMPtec Europe GmbH and fill out the form. Take care to include a short detailed description of the observed problem or failure and to include the product identification Information (Name of product, Product number and Serial number). If a delivery includes more than one product, fill out the above information in the RMA Request form for each product.

2. Send the completed RMA-Request form to the fax or email address given below at JUMPtec Europe GmbH. JUMPtec will provide an RMA-Number.

JUMPtec Europe
GmbH RMA Support
Phone: +49 (0) 821 4086-0
Fax: +49 (0) 821 4086 111
Email: service@JUMPtec.com

3. The goods for repair must be packed properly for shipping, considering shock and ESD protection.

Goods returned to JUMPtec Europe GmbH in non-proper packaging will be considered as customer caused faults and cannot be accepted as warranty repairs.

4. Include the RMA-Number with the shipping paperwork and send the product to the delivery address provided in the RMA form or received from JUMPtec RMA Support.

Appendix A: List of Acronyms

API	Application Programming Interface
BIOS	Basic Input Output System
BMC	Base Management Controller
BSP	Board Support Package
CAN	Controller-area network
Carrier Board	Application specific circuit board that accepts a COM Express ® module
COM	Computer-on-Module
Compact Module	COM Express® 95x95 Module form factor
CNTG	Computer Network Transaction Groug
DDC	Display Data Control
DDI	Digital Display Interface –
DIMM	Dual In-line Memory Module
Display Port	DisplayPort (digital display interface standard)
DMA	Direct Memory Access
DRAM	Dynamic Random Access Memory
DVI	Digital Visual Interface.
EAPI	Embedded Application Programming Interface
ECC	Error Checking and Correction
EEPROM	Electrically Erasable Programmable Read-Only Memory
eDP	Embedded Display Port
EMC	Electromagnetic Compatibility (EMC)
ESD	Electro Sensitive Device
Extended Module	COM Express® 155mm x 110mm Module form factor.
FIFO	First In First Out
FRU	Field Replaceable Unit
Gb	Gigabit
GBE	Gigabit Ethernet
GPI	General Purpose Input
GPIO	General Purpose Input Output
GPO	General Purpose Output
GPU	Graphics Processing Unit
HBR2	High Bitrate 2
HDA	High Definition Audio (HD Audio)
HD/HDD	Hard Disk /Drive
HDMI	High Definition Multimedia Interface
HPM	PICMG Hardware Platform Management specification family

I2C	Inter integrated Circuit Communications
IOL	IPMI-Over-LAN
IOT	Internet of Things
IPMI	Intelligent Platform Management Interface
KCS	Keyboard Controller Style
KVM	Keyboard Video Mouse
LAN	Local Area Network
LPC	Low Pin-Count Interface:
LVDS	Low Voltage Differential Signaling –
M.A.R.S.	Mobile Application for Rechargeable Systems
MEI	Management Engine Interface
Mini Module	COM Express® 84x55mm Module form factor
MTBF	Mean Time Before Failure
NA	Not Available
NC	Not connected
NCSI	Network Communications Services Interface
PCI	Peripheral Component Interface
PCIe	PCI-Express
PECI	Platform Environment Control Interface
PEG	PCI Express Graphics
PICMG®	PCI Industrial Computer Manufacturers Group
PHY	Ethernet controller physical layer device
Pin-out Type	COM Express® definitions for signals on COM Express® Module connector pins.
PSU	Power Supply Unit
RMS	Root Mean Square
RTC	Real Time Clock
SAS	Serial Attached SCSI – high speed serial version of SCSI
SATA	Serial AT Attachment:
SCSI	Small Computer System Interface
SEL	System Event Log
ShMC	Shelf Management Controller
SMBus	System Management Bus
SOIC	Small Outline Integrated Circuit
SOL	Serial Over LAN
SPI	Serial Peripheral Inteface
SSH	Secure Shell

TPM	Trusted Platform Module
UART	Universal Asynchronous Receiver Transmitter
UEFI	Unified Extensible Firmware Interface
UHD	Ultra High Definition
USB	Universal Serial Bus
VGA	Video Graphics Adapter
VLP	Very Low Profile
WDT	Watch Dog Timer
WEEE	Waste Electrical and Electronic Equipement (directive)

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About JUMPtec is a global leader in Embedded Computing Technology (ECT). JUMPtec offers a combined portfolio of secure hardware, middleware and services for Internet of Things (IoT) and Industry 4.0 applications. With its standard products and tailor-made solutions based on highly reliable state-of-the-art embedded technologies, JUMPtec provides secure and innovative applications for a variety of industries. As a result, customers benefit from accelerated time-to-market, reduced total cost of ownership, product longevity and the best fully integrated applications overall.

For more information, please visit: http://www.congatec.com

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